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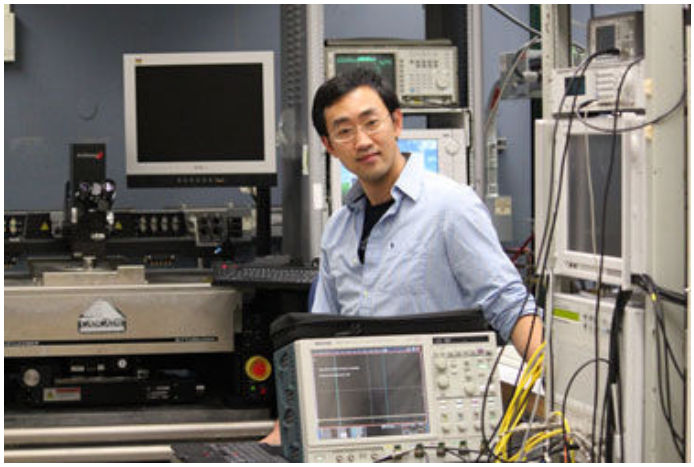
CNT arrays make record-breaking transistors

Single-walled carbon nanotubes could be ideal for replacing silicon in applications such as thin-film transistors and high-performance logic devices thanks to their exceptional electronic and mechanical properties. However, researchers will need to be able to fabricate dense, aligned arrays of electronically pure nanotubes if real-world devices are to see the light of day. A team at IBM has now succeeded in doing just this by using the so-called Langmuir-Schaefer method to assemble semiconducting nanotube arrays with a surface density of more than 500 tubes/micron. Transistors made using these nanotubes have record-breaking properties, with drive current densities of more than 120 μA/m, transconductances of greater than 40 μS/m and on/off ratios of more than 1000.



(http://images.iop.org/objects/ntw/news/12/2/4/image1.jpg)
Qing Cao (http://images.iop.org/objects/ntw/news/12/2/4/image1.jpg)

The features in conventional microelectronic circuits are getting ever smaller and will soon reach the limit imposed by the fundamental properties of silicon. Scientists hope that carbon nanotubes – which are essentially rolled up sheets of graphite, just nanometres in diameter – might one day be used to replace silicon in electronic circuits.

It is possible to make dense aligned arrays of carbon nanotubes through techniques like chemical vapour deposition on crystalline substrates. However, this approach produces a mix of metallic and semiconducting tubes and it is difficult to remove the metallic tubes without degrading the performance of the semiconducting ones. Metallic and semiconducting nanotubes can also first be separated out in solution and then assembled into aligned arrays using external electric fields or shear forces, but unfortunately these methods produce arrays with a density of just 50 tubes/μm. Such a density is far too low, and the current output from these arrays can in no way compete with silicon-based devices for high-performance applications.

(http://images.iop.org/objects/ntw/news/12/2/4/image2.jpg)
False-coloured SEM image (http://images.iop.org/objects/ntw/news/12/2/4/image2.jpg)

A team led by Wilfried Haensch at the IBM TJ Watson Research Centre in New York employed the Langmuir-Schaefer technique – a versatile way to make dense arrays of 1D nanomaterials, like single-walled carbon nanotubes or nanowires. This method can also be scaled up and so might be used to fabricate nanostructured arrays on whole wafers.

"The method we used can be understood using a 'logs-on-a-river' analogy," explained team member Qing Cao. "After dispersing nanotubes on the surface of water, they spread out to form a monolayer – thanks to surface tension – and orient themselves randomly. They are then compressed and the applied pressure aligns them all in the same direction, with the pitch being self-limited by nanotube diameter."

The arrays produced are made up of 99% semiconducting nanotubes.

"Silicon is expected to run out of steam in a few years from now, so one of IBM's targets is to replace silicon with carbon nanotubes for high-performance logic electronics since nanotube transistors could run chips at one-third the power and three times faster than silicon devices," Cao told *nanotechweb.org*. "Our work is an important step towards this goal."

Spurred on by their results, the IBM researchers are now busy improving the electrical contact between nanotube arrays and metal electrodes in the transistor devices they made. They are also looking at further optimizing the nanotube electronic type separation and reducing interface traps for making more uniform devices.

The current work is detailed in *Nature Nanotechnology*.

About the author

Belle Dumé is contributing editor at *nanotechweb.org*.