A nanometer leap to trillions of transistors

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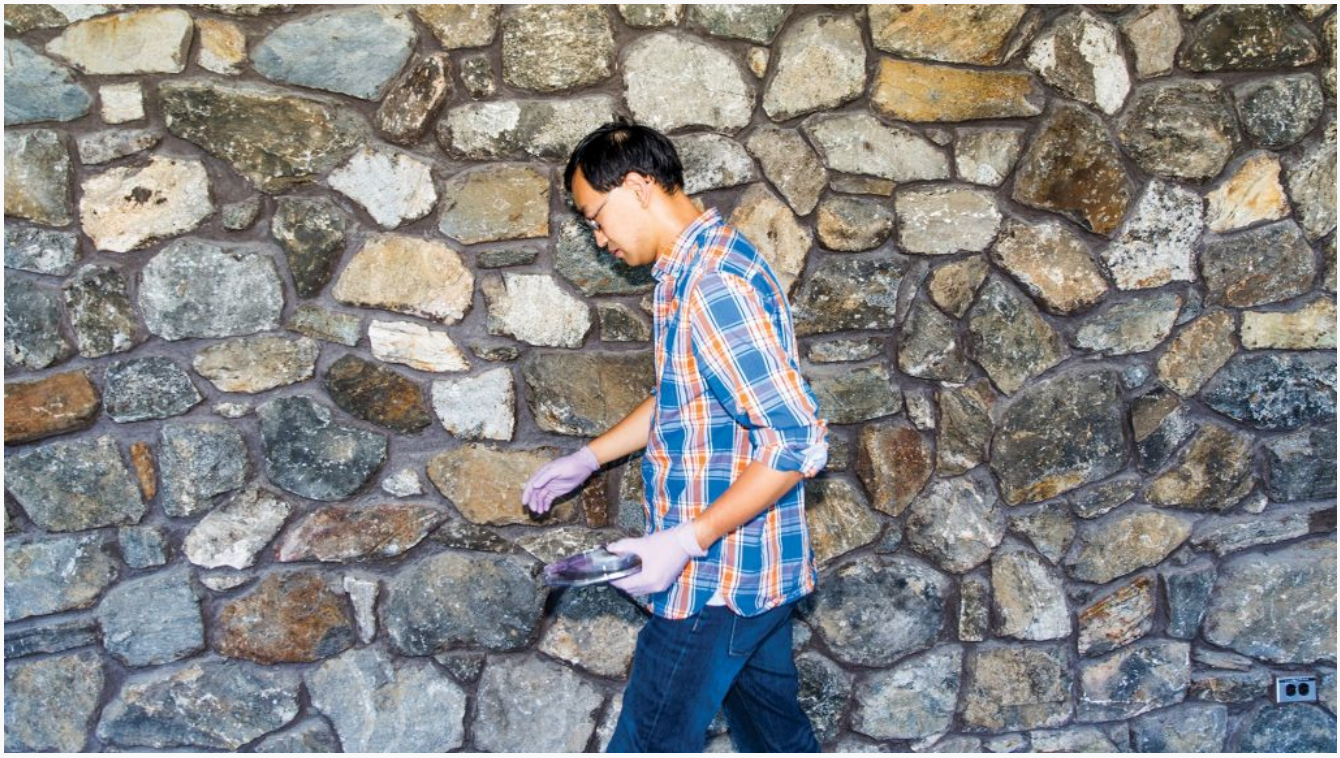
IBM Research scientist Qing Cao develops way to link carbon nanotubes

Scientists and engineers don't need to wear clapboards in Times Square declaring "The end of Moore's Law is near." They all know that silicon-based computer chips will soon cease to improve in speed and shrink in size. One of those scientists, IBM's Qing Cao may have found the alt-silicon answer in carbon nanotubes – rolled-up sheets of carbon that can better-conduct electrical signals at a much smaller scale than silicon.

Cao, who was recognized as a Pioneer Under 35 by *MIT Technology Review* this year, figured out a way to align CNTs together, and then fuse them to tiny metal connector wires. This means they could be scaled out to the size of today's silicon chips, and eventually replace them in tomorrow's computers. Cao explained how he accomplished aligning nanotubes into arrays and then welding metal atoms to the end of a four-atom wide nanotube at this week's *TR*'s EmTech in Cambridge, MA. I caught up with Cao to get a nano-peek at his talk.*



Qing Cao, IBM Research (photo credit: MIT Technology Review)

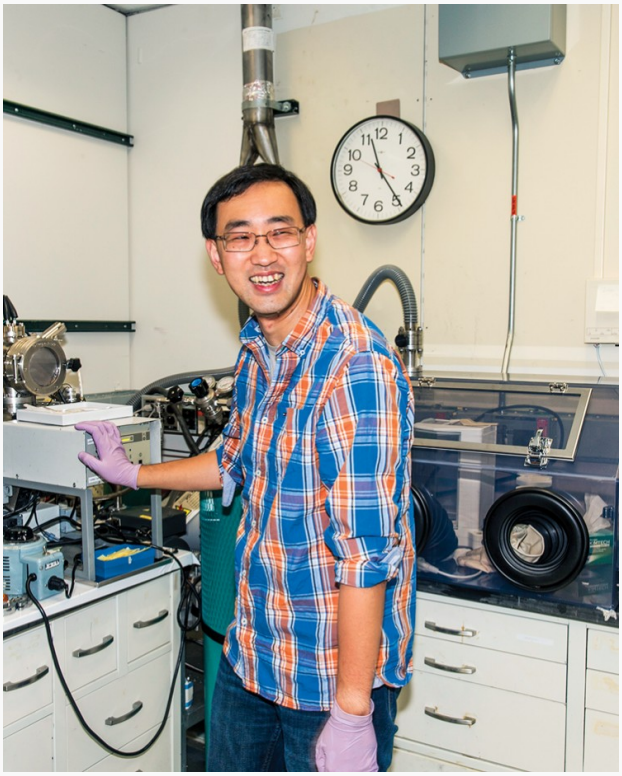
What is Silicon's limit and how do CNTs go beyond that limit?

Qing Cao: Silicon chips already hold billions of transistors at 22 nm. These are the kinds of chips in today's servers. And we've shown that 7 nm is possible. But Silicon's capability ends at around 5 or 6 nm as it hits the wall of quantum mechanics. Carbon nanotubes however, with its intrinsically small size – about 1 nm, or just four atoms wide – allows us to get to 5 nm node or beyond. At this scale, CNT transistors could operate twice as fast compared to silicon, while consuming less than half of the power.

Why haven't we been able to build CNT chips, yet?

QC: When we move to smaller devices, the connectors have to shrink at the same time. But the reduction of metal connector size, down to sub-10 nm, sharply increases the resistance and thus kills the device performance. We –

my team at the Thomas J Watson Research Center and I – developed a way to connect the end of the CNTs to a Molybdenum wire through strong chemical bonds, and verified, in this case, that the reduction of the connector dimension will not compromise device performance, even if the size of the metal connectors shrank to just 40 atoms wide or even smaller.



Qing Cao, IBM Research (photo credit: MIT Technology Review)

After solving the connector problem, we still need a CNT wafer to build CNT chips. My team has developed a way to self-assemble nanotubes into side-by-side aligned arrays on wafers. Being able to assemble CNT arrays onto a wafer and then connect them with tiny metallic wires with minimal resistive loss will mean smaller chips at faster speeds than silicon – and the continuation of Moore's Law.

When do you think these chips make it into our computers and devices?

QC: I think such nanotube devices will emerge in products in the next 10-15 years and help to sustain Moore's Law for at least the next 20 years. Eventually, we want to pack 1 trillion transistors onto a processor (that's more than the number of stars in the Milky Way!)