Scaling of Device Variability and Subthreshold Swing in Ballistic Carbon Nanotube Transistors

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In field-effect transistors, the inherent randomness of dopants and other charges is a major cause of device-to-device variability. For a quasi-one-dimensional device such as carbon nanotube transistors, even a single charge can drastically change the performance, making this a critical issue for their adoption as a practical technology. Here we calculate the effect of the random charges at the gate-oxide surface in ballistic carbon nanotube transistors, finding good agreement with the variability statistics in recent experiments. A combination of experimental and simulation results further reveals that these random charges are also a major factor limiting the subthreshold swing for nanotube transistors fabricated on thin gate dielectrics. We then establish that the scaling of the nanotube device uniformity with the gate dielectric, fixed-charge density, and device dimension is qualitatively different from conventional silicon transistors, reflecting the very different device physics of a ballistic transistor with a quasi-one-dimensional channel. The combination of gate-oxide scaling and improved control of fixed-charge density should provide the uniformity needed for large-scale integration of such novel one-dimensional transistors even at extremely scaled device dimensions.

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I. INTRODUCTION

Single-walled carbon nanotubes (SWNT) exhibit many remarkable properties as a one-dimensional (1D) nanomaterial. They are particularly attractive for advanced high-performance logic devices, due to their intrinsic ultrathin body and ballistic transport of carriers at room temperature, potentially leading to better performance or lower power consumption than conventional silicon technologies [1–4]. Recent breakthroughs in the purification and assembly of carbon nanotubes [5–9], and circuit-level demonstrations using SWNT transistors up to a fully functional computer [10], suggest that nanotube-based nanoelectronics may become a practical technology to be incorporated into next-generation microprocessors.

Any electronic device contains some random charges introduced either intentionally as dopants or unintentionally as traps or fixed charges, causing significant random variability. For large-scale integration, device-to-device uniformity is as critical as the performance of individual devices, as it affects both circuit performance and yield. Therefore, variability statistics have been studied extensively for conventional semiconductor devices in both experiments [11–13] and in simulations based on either classical or semiclassical device models [14–18] or first-principles quantum mechanics [19,20]. However, quasi-1D devices like nanotube transistors could demonstrate very different behaviors due to some fundamental issues. In ballistic nanotube field-effect transistors (FETs), even a single charge can affect the device operation. If it is close enough to the nanotube, it can shift the threshold voltage (V_T) at which the device turns on by several hundred millivolts, and degrade the subthreshold swing (SS), i.e., the turn-on sharpness of the device [21,22]. Because of the disproportionate effect of nearby charges, we may expect quite different variability statistics for nanotube FETs, yet little is known about how the variability of such devices scales with device dimensions or gate dielectrics. Recent experiments have begun to address this, measuring a large number of devices built on individual nanotubes [23], and analyzing them phenomenologically by adapting a model for conventional silicon FETs. However, we cannot expect such an approach to accurately predict variability scaling over a wide range of conditions. In particular, it is most appropriate when the charge density is high, while for technology we are more interested in the device behaviors with the presence of low densities of charges, where effects from the discreteness of charges are more significant.

To provide a more accurate and predictive description of the device variability caused by discrete random charges, we build a microscopic Monte Carlo model for transmission through ballistic nanotube FETs. Based on this model, the V_T variability characteristics observed in the experiments can be well reproduced. Comparison with the experiment further indicates that random fixed charge is also a major but previously unrecognized factor limiting both the average value of SS and its uniformity across nominally identical SWNT transistors. The V_T variability of ballistic SWNT FETs can be systematically improved by minimizing the density of the random fixed charges (n_{SS}), by reducing that gate-oxide thickness (t_{ox}), or by using an

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oxide with a higher dielectric constant (κ). However, we find that the V_T variability improvement upon scaling these parameters can deviate dramatically from the trend predicted in conventional bulk-device models, especially in the low-n_{SS} regime, due to the 1D nature of nanotubes. We also find a very different channel-length scaling behavior than for conventional transistors. If the n_{SS} is low, the reduction of device length actually improves the device variability, a trend opposite to that of conventional FETs. Finally, we show that building transistors by incorporating multiple SWNTs in parallel as the channel is a particularly effective method to enhance the V_T uniformity, due to synergetic effects from the nonlinearity of subthreshold current and the broken symmetry for charge polarity in unipolar nanotube transistors.

II. MODEL

Our model system for simulation is schematically illustrated in Fig. 1(a). It is microscopic, in the sense that we include random charge positions and potential variations on a scale much smaller than the diameter of the nanotube. We use a standard back-gated geometry, and assume for simplicity that the gate oxide and nanotube are capped with a thick protective layer of the same oxide. (In the experiments, there is actually air above the gate oxide.) Positive fixed charges are randomly distributed with density n_{SS} at the interface between gate oxide and capping oxide, since previous work found that this was the dominant source of threshold voltage shift [23]. The interface positions are discretized at a grid resolution of 1 Å over an area of 1 μm by 1 μm. At each position, a fixed charge is randomly included with probability $n_{SS} \times (1\ \text{Å})^2$. The radius of the nanotube (r) is set as 0.6 nm, the average extracted from the experiment [23]. The nanotube band structure is approximated by the usual p-orbital tight-binding model [24], with the nearest-neighbor overlap integral being $\gamma_0 = 2.7$. This gives a band gap (E_g) of $E_g = \gamma_0 \alpha_0 / r$, where $\alpha_0 = 1.42$ Å is the carbon—carbon bond length. The total electrostatic potential $V(z)$ from all of the fixed charges in the simulated area is calculated using Poisson's equation at each point z along the axis of the nanotube with the gate held at ground potential, using the image-charge method. Charging of the nanotube itself is not included since it is negligibly small in the subthreshold regime of gate voltage considered here. The actual potential when the gate is held at voltage V_{GS} is then $E + eV_{GS}$. Here our focus is the effect of fixed charge on the channel, so we assume zero barrier and neglect fringe fields at the contacts.

Figure 1(b) shows a typical simulated band-edge profile along a tube with an r of 0.6 nm and a E_g of 0.64 eV [25], for positive fixed charges of density $n_{SS} = 5 \times 10^{12}\ \text{cm}^{-2}$ and applied gate bias $V_{GS} = 0$. The charge sign and density are extracted from the experiment based on the conventional silicon-FET model [23]. The nanotube is intrinsic, i.e., no chemical doping is included. The band-edge profile exhibits a dramatic and complex variation along the axis of the nanotube resulting from the modulation of electrostatic potential by fixed charges. The bands are shifted on average by several eV. In addition, there are large variations along the length of the device, including both sharp dips and fluctuations over a range of length scales.

From the band-edge profile in Fig. 1(b), we see that at a given energy (E) there are regions where an electron or hole can propagate, and other regions where E lies within the band gap and the wave function is decaying. At a given energy E, there could be many decaying regions along the $V(z)$ profile. Through each individual decaying region i, we calculate the transmission using the Wentzel-Kramers-Brillouin (WKB) approximation as

$$\ln T_i = -\frac{4}{3bV_\pi} \int_{z_s}^{z_f} \sqrt{\frac{E_g^2}{4} - [E - eV(z)]^2} dz, \qquad (1)$$

where $b = 0.144$ nm is the carbon—carbon bond length, $V_\pi = 2.5$ eV is the tight-binding parameter, and e is elementary charge [26]. Z_s and Z_f define the starting and the ending points for the ith decaying region, where the E is within the band gap of the nanotube. Since here we study only the exponentially varying characteristics of the subthreshold regime, WKB provides sufficient accuracy together with great simplicity and transparency. Neglecting interference effects, the transmission through the entire channel (T_{ch}) is [27]

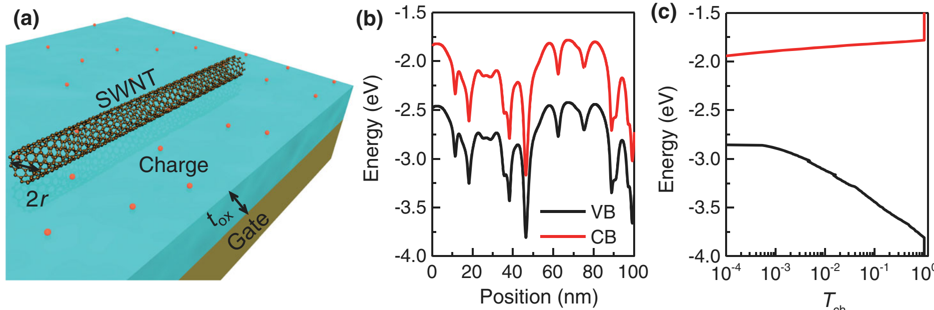

FIG. 1 (a) Schematic illustration of the microscopic model we built for the simulation. (b),(c) A representative channel-region band diagram [part (b)] and the calculated T_{ch} as a function of energy [part (c)] for a ballistic FET built on a 100-nm-long nanotube lying on top of 10-nm-thick SiO_2 with a surface charge density of $5\times10^{12}\text{cm}^{-2}$ as gate dielectric. VB, valence band edge; CB, conductance band edge.

$$T_{\mathrm{ch}} = \left[\left(\sum_i \frac{1-T_i}{T_i}\right) + 1\right]^{-1}. \tag{2}$$

The relationship between energy and T_{ch} for this particular simulated device is depicted in Fig. 1(c). There is a dramatic asymmetry between the p branch and the n branch, as also seen in earlier simulations for single charges using the nonequilibrium Green's function method [21]. This is because a potential dip from a positive charge is a barrier for holes but only a potential well for electrons. Here we focus exclusively on the polarity showing the larger effect: the p channel for positive charges or the n channel for negative charges. (This is also the case for which data on variability are available.) The drain-to-source current (I_{DS}) is then

$$I_{\mathrm{DS}} = \frac{4e}{h}\int_{-\infty}^{+\infty}\left[F(E) - F(E + eV_{\mathrm{DS}})\right]T_{\mathrm{ch}}(E + eV_{\mathrm{GS}})dE, \tag{3}$$

where h is the Plank constant, $F(E)$ is the Fermi function, V_{DS} is the applied source-drain bias, and $T_{\mathrm{ch}}(E + V_{\mathrm{GS}})$ includes the uniform shift of T_{ch} curve as plotted in Fig. 1(d) by applied V_{GS}. Here we assume perfect Ohmic contacts for the valence band, and we neglect current resulting from the tunneling of electrons into the conduction band. Based on the calculated device IV characteristics, the simulated V_T is defined at the V_{GS} required to reduce the I_{DS} to 1% of its maximum value in the fully on state, and the corresponding subthreshold swing $\mathrm{SS} = [d\ln(I_{\mathrm{DS}})/dV_{\mathrm{GS}}]^{-1}$ is evaluated at V_T.

III. RESULTS AND DISCUSSION

We first validate our model against our previous experimental results [23]. Figures 2(a) and 2(b) depict the collections of nominal identical single-tube transistors made in an experiment on a SiO_2 (dielectric constant $\varepsilon_r = 3.9$) gate dielectric with two different t_{ox}. Details of their fabrication process and their extracted average V_T as well as $\sigma(V_T)$ have been described before [23]. A significant shift of average V_T and a reduction of its standard deviation $[\sigma(V_T)]$ is observed with the decrease of t_{ox} from 15 to 2 nm. In simulation, for each case, 300 nominally identical devices are generated to calculate the average V_T and $\sigma(V_T)$. To reproduce the experimental geometry, each nanotube is randomly orientated between two parallel contacts, with the tube length up to 600 nm [23]. The comparison between experimental and simulated values is shown in Figs. 2(c) and 2(d). Figure 2(c) shows the scaling of average V_T with t_{ox}. The experimental results are well described by a conventional model neglecting the discreteness of charge, assuming $n_{\mathrm{SS}} = 5 \times 10^{12}$ cm^{-2}. For the same n_{SS}, the full simulations give a somewhat larger threshold shift, by 200–400 meV, but overall the behavior is well described by the conventional bulk model, including the linear scaling with t_{ox}. This is perhaps not surprising, since we are looking at an average value, and the neglect of charge discreteness in the conventional model is itself a sort of averaging.

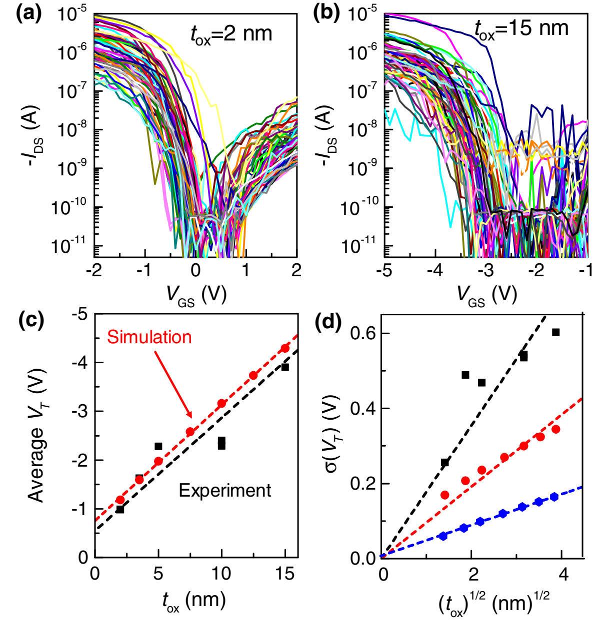

FIG. 2. (a),(b) Subthreshold plots of transistors made on individual nanotubes using 2-nm [part (a)] and 15-nm [part (b)] SiO_2 as gate dielectric. Applied V_{DS} is -0.5 V. (c) Comparison of the average threshold voltage V_T extracted from the experiment (black squares) and the simulation (red circles) as a function of SiO_2 thickness t_{ox} from 2 to 15 nm. Simulation is for $n_{\mathrm{SS}} = 5 \times 10^{12}$ cm^{-2}. Dashed lines represent linear fittings to the data. (d) Standard deviation of threshold voltage $\sigma(V_T)$ as calculated from the experiment (black squares), conventional bulk FET model (blue diamonds), and the full simulation (red circles) as a function of $t_{\mathrm{ox}}^{1/2}$. Dashed lines are linear fits to the data through the origin.

On the other hand, the discreteness is essential for determining the variability, especially for SWNT devices. For conventional silicon FETs, V_T is well described by the average potential of the channel, with discreteness entering only via random variations in the total number of charges. In Fig. 2(d), we compare $\sigma(V_T)$ from the experiment, our full simulation results, and the conventional bulk model where V_T for each nanotube is determined by the average potential along the nanotube axis. The variability in the average potential scales as $t_{\mathrm{ox}}^{1/2}$. In contrast, the full simulation gives some deviation from $t_{\mathrm{ox}}^{1/2}$, and more importantly, more than twice as large a variability. This reflects the reality that carriers cannot pass around local barriers in a quasi-1D semiconductor like SWNTs, and thus local fluctuations are as important as the average potential in determining V_T. Indeed, a single charge placed right at

the nanotube-oxide interface can significantly deform the transmission curve in a quantitatively similar fashion as what has been reported in earlier calculations performed with the more rigorous nonequilibrium Green's function approach [21], and shift V_T by ~250 mV for a 100-nm channel device built on 10-nm-thick SiO_2 gate dielectric (see Supplemental Material, Fig. S1 [28]).

The effect of a single charge decreases rapidly with its increasing distance from the nanotube. Yet for the n_{SS} level in Fig. 2, the overall shift of V_T is dominated by the collective effect of many charges at some distance from the nanotube. If we only had fixed charges or dopants right on the surface of nanotubes, even at an impractically high doping concentration of one dopant in every 1000 carbon atoms (10 times higher than the degenerate doping level for semiconducting nanotubes [29]), the change of either average V_T or $\sigma(V_T)$ against t_{ox} observed in the experiment could not be reproduced in the simulation (see Supplemental Material, Fig. S2 [28]). In contrast, if we assume a fixed charge distributed over the gate-oxide surface, the simulated $\sigma(V_T)$ agrees well with the experiment, as shown in Fig. 2(d). We note that the magnitude of the simulated $\sigma(V_T)$ is still almost 50% lower than the experimental result. However, this discrepancy is caused in large part by the simplified space-filling dielectric in our simulations, which screens the charge more effectively than in the experiment, where nanotubes have oxide below but air ($\varepsilon_r = 1$) above. This does not affect the potential within the conventional sheet-charge model, which describes well the average V_T; but the air-exposed geometry gives larger local fields, and hence a larger variability. Based on the good agreement between the experiment and the simulation, we conclude that this microscopic model is reliable for characterizing and predicting the variability of quasiballistic SWNT transistors caused by random fixed charges on the gate-oxide surface.

Figures 2(a) and 2(b) also reveal that the average sharpness of the turn-on with gate voltage is only marginally improved with the reduction of t_{ox} from a small value of 15 nm to the extreme case of merely 2 nm. This is contrary to the large improvement expected from standard models, and represents an important issue that has not been reported before. The sharpness of turn-on is a critical issue for device power consumption, and is characterized by the subthreshold swing SS. An average SS above 200 mV/dec is observed for devices made on all five different t_{ox}. This is much larger than the theoretical limit for thermally activated on and off switching, $\mathrm{SS} = 60$ mV/dec. Such deviations have generally been attributed to influences from interface capacitance (C_{it}) caused by traps, or from Schottky barriers at the contacts [26,30–32]. However, an examination of the scaling tells a different story. The effect from C_{it} diminishes with the increase of C_i and the device SS is proportional to $1 + C_{it}/C_i$. C_i for single-tube transistors is calculated according to

$$C_i = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln(t_{ox}/r + 1)}, \tag{4}$$

where ε_0 is the vacuum permittivity [33]. The effect from the Schottky barrier at the contacts is predicted to decrease proportionally with the square root of t_{ox} as the barrier width becomes smaller with thinner dielectric [26]. As shown in Figs. 3(a) and 3(b), the adoption of gate oxide with smaller t_{ox} indeed improves the SS following these trends, especially for transistors built on thick oxide. However, for both cases, the measured SS is extrapolated to saturate at 160–180 mV/dec, even with infinitely small t_{ox}, which indicates that some other factor dominates the average SS of nanotube transistors built on thin oxide.

We saw in Fig. 1(c) that, in addition to shifting V_T, the presence of random charges degrades the device SS as well. This effect comes primarily from charges located almost right under the nanotube, and the effect is insensitive to t_{ox} as the change of t_{ox} even to the extreme case of 2 nm has only a modest effect on the potential arising from those very nearby charges (see Supplemental Material, Fig. S1 [28]). This observation suggests that those randomly distributed fixed charges on the oxide surface could also have an unexpected but large impact on the average SS

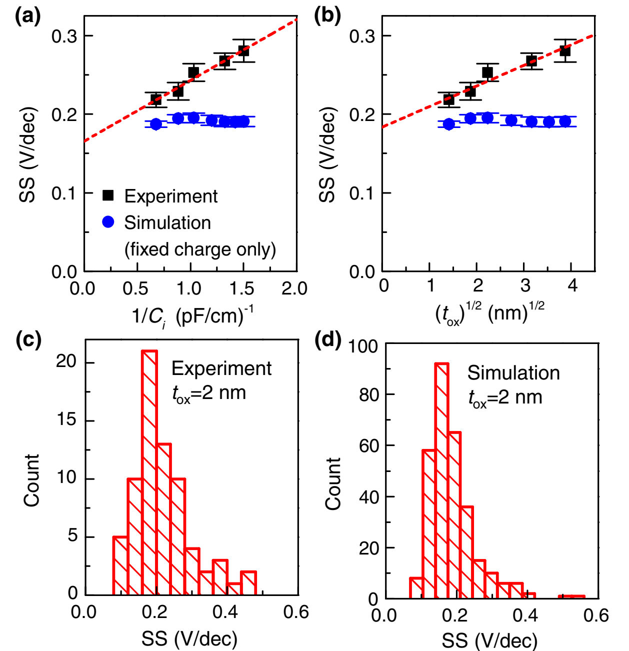

FIG. 3 (a),(b) Black squares show the measured subthreshold swing SS as a function of the reciprocal of gate capacitance C_i [part (a)] and the square root of oxide thickness t_{ox} [part (b)]; and blue circles show the simulation result, which includes only the contribution from random fixed charges and assumes ideal contacts and negligible capacitance from interface traps. Error bars correspond to the standard error. (c),(d) The histograms showing the distribution of SS measured from the experiment [part (c)] and obtained from the simulation [part (d)] for nanotube devices made with 2-nm SiO_2 gate dielectric.

and its variability for nanotube transistors built on scaled dielectrics where impacts from C_{it} and the Schottky barriers are minimized. The simulated average SS with degradation from the thermal limit purely caused by such fixed charges ($n_{SS} = 5 \times 10^{12}$ cm^{-2}, assuming all devices form perfect Ohmic contacts with source and drain electrodes and there is no interface capacitance from traps) are then plotted in Figs. 3(a) and 3(b) for comparison. Since the influence from either the interface capacitance or the Schottky barrier at contacts is not included in the simulation, their impact on the average SS is virtually independent of t_{ox}, and is quantitatively close to the residual value extracted in the experiment for devices with t_{ox} approaching zero. Figures 3(c) and 3(d) further compare the distribution of SS for devices built on a 2-nm SiO_2 gate dielectric extracted from the experiment and obtained from the simulation. The good agreement in both values and the shape of the distribution suggest that these randomly distributed fixed charges are the major contributor to the degradation of SS for nanotube devices built on scaled dielectrics, a factor that has not been previously appreciated in this field. Reducing n_{ss} is then critical to improving the average SS of scaled nanotube transistors and keeping their performance advantage in the subthreshold regime compared to bulk silicon devices.

On the other hand, the V_T variability of SWNT transistors can be improved through either further reducing the n_{SS} with better passivation or scaling down the gate dielectric. To determine the best practice, it is imperative to determine the change of $\sigma(V_T)$ upon the scaling of these parameters. We first consider the scaling of t_{ox}. As shown in Fig. 2(d), $\sigma(V_T)$ is approximately proportional to the square root of t_{ox} if the n_{SS} is high. To find out whether this relationship is valid for the whole spectrum of n_{SS}, we calculate the effect of t_{ox} scaling on the device V_T variability under different n_{SS}, and summarize the results in Fig. 4(a). Here we assume that all nanotubes are perfectly aligned with their tube lengths equals device L_{ch}. Figure 4(a) shows that in the low-n_{SS} regime, the dependence of $\sigma(V_T)$ on t_{ox} becomes much weaker, and only a marginal improvement can be achieved from reducing t_{ox}.

The crossover between regimes in Fig. 4(a) has a very odd feature—for the thinnest oxide, reducing the charge by an order of magnitude, from 10^{12} to 10^{11} cm^{-2}, has virtually no effect on $\sigma(V_T)$. To understand this, we plot the actual V_T distributions in Figs. 4(b) and 4(c). If n_{SS} is high, the potential at any point on the tube typically reflects the effect from a statistical number of charges nearby. This leads to a nearly Gaussian distribution of V_T, scaling as $t_{ox}^{1/2}$, as we observed previously in the experiment [23]. However, if n_{SS} is very low, V_T can be dominated by a few charges or even a single charge very near the tube, leading to a non-Gaussian distribution of V_T. Moreover, the V_T variation in this case exhibits a much weaker dependence

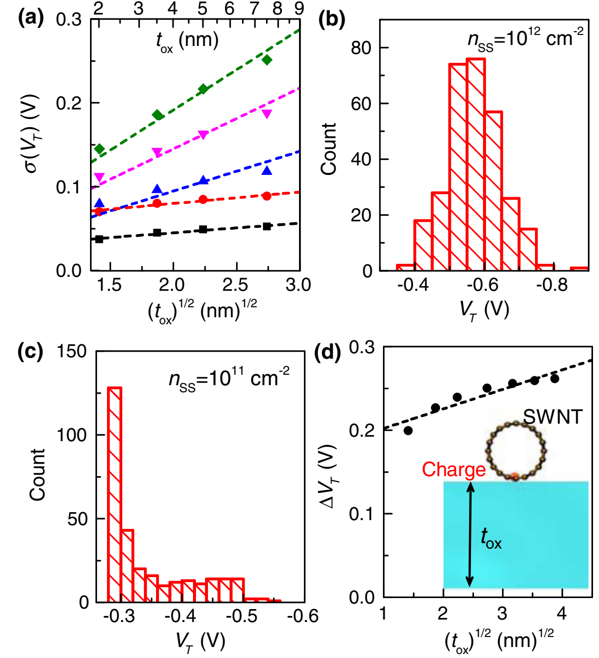

FIG. 4 (a) Simulated $\sigma(V_T)$ as a function of the t_{ox} for n_{SS} from 1×10^{13} cm^{-2} (green diamonds), 5×10^{12} cm^{-2} (magenta down triangles), 1×10^{12} cm^{-2} (blue up triangles), 1×10^{11} cm^{-2} (red circles), to 2×10^{10} cm^{-2} (black squares), from top to bottom, with t_{ox} plotted on a square-root scale. Dashed lines serve as a visual guide to mark their different trends. (b),(c) Histograms showing the V_T distributions for nominal identical SWNT FETs simulated with a L_{ch} of 100 nm on 2-nm-thick SiO_2 gate dielectrics bearing a n_{SS} of 10^{12} cm^{-2} [part (b)] and 10^{11} cm^{-2} [part (c)], respectively. (d) The shift of the V_T caused by a single charge placed at the nanotube-oxide interface and midway between the source and drain electrodes as a function of the square root of t_{ox}. Inset, schematic showing the t_{ox} and the location of the charge. Dashed black line represents a linear fitting.

on t_{ox} as illustrated in Fig. 4(a), and even more for a single charge as shown in Fig. 4(d).

Another way to improve device uniformity is to adopt gate dielectrics with larger ε_r for better screening of charges. We perform simulations for sets of nominal identical devices built on SiO_2 ($\varepsilon_r = 3.9$),Al_2O_3 ($\varepsilon_r = 9$), and HfO_2 ($\varepsilon_r = 14$) with L_{ch} of 100 nm. As shown in Figs. 5(a) and 5(b), $\sigma(V_T)$ varies inversely with ε_r, making the adoption of high-κ dielectric a particularly effective way to reduce the variability of ballistic SWNT FETs. This scaling is very intuitive, and our simulations confirm that it is valid for different t_{ox} over a wide range of n_{SS}. For an extremely scaled device built on 2-nm HfO_2 as gate dielectric, even with a high n_{SS} level of 1×10^{13} cm^{-2}, $\sigma(V_T)$ below 50 mV can be achieved for single-tube devices built on nanotubes with identical band gaps. In this regime, the variability caused by nanotube-diameter variations could become significant relative to other factors, as its effect cannot be reduced with gate-dielectric engineering. The range of nanotube diameters for our current

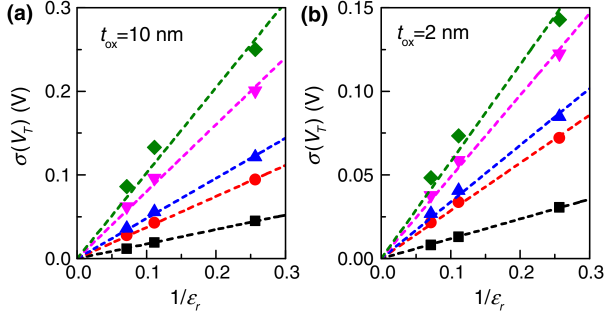

FIG. 5. Simulated $\sigma(V_T)$ as a function of the reciprocal of ε_r for devices built on 10-nm [part (a)] or 2-nm [part (b)] thick oxides with the n_{SS} varying from 1×10^{13} cm^{-2} (green diamonds), 5×10^{12} cm^{-2} (magenta down triangles), 1×10^{12} cm^{-2} (blue up triangles), 1×10^{11} cm^{-2} (red circles), to 2×10^{10} cm^{-2} (black squares), from top to bottom. The device L_{ch} is 100 nm. Solid lines represent linear fittings to the data through the origin.

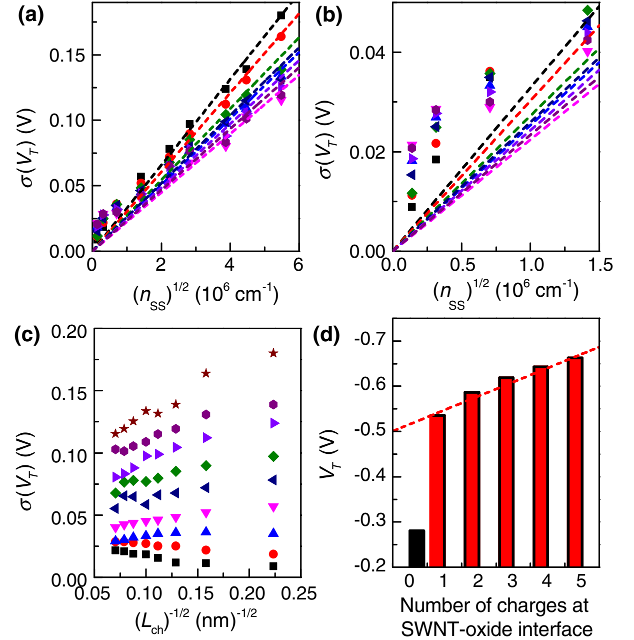

FIG. 6 (a) Simulated $\sigma(V_T)$ as a function of the square root of n_{SS} for SWNT transistors with L_{ch} of 20 nm (black squares), 40 nm (red circles), 60 nm (green diamonds), 80 nm (navy left triangles), 100 nm (blue up triangles), 130 nm (violet right triangles), 160 nm (purple hexagons), and 200 nm (magenta down triangles). Dashed lines represent linear fittings to the data though the origin. (b) Enlargement of the low-density regime of (a) showing strong deviations from $n_{SS}^{1/2}$ scaling. (c) Simulated $\sigma(V_T)$ as a function of the reciprocal of the square root of L_{ch} for n_{SS} of 3×10^{13} cm^{-2}, 2×10^{13} cm^{-2}, 1.5×10^{13} cm^{-2}, 8×10^{12} cm^{-2}, 5×10^{12} cm^{-2}, 2×10^{12} cm^{-2}, 5×10^{11} cm^{-2}, 10^{11} cm^{-2}, and 5×10^{10} cm^{-2}, from top to bottom. (d) The calculated V_T as a function of the number of fixed charges residing right at the nanotube-oxide interface and evenly distributed between two ends of the nanotube for 100-nm L_{ch} devices built on 10-nm SiO_2 gate dielectric. The red dashed line represents a linear fit to the cases where there is at least one nearby fixed charge.

as-prepared nanotube solution leads to a $\sigma(V_T)$ up to 90 mV [23]. However, recent progress in both selective growth and high-efficiency sorting techniques suggests it is possible to keep this variability under better control with a narrower distribution of the nanotube diameter [34–37].

For the best-possible uniformity, n_{SS} should also be reduced with better passivation schemes [38], in parallel with gate-dielectric scaling. Figure 6 shows the interplay between n_{SS} and L_{ch} for devices made on 10-nm HfO_2 gate dielectric, illustrating the novel scaling. In the high-n_{SS} regime, as discussed above, V_T is determined by both local and long-range fluctuations of the potential. Increasing n_{SS} linearly increases the shift of the average potential, as expected. For local fluctuations, since n_{SS} is high, there is at least one fixed charge very close to the nanotube for each device. Then the linear relationship between V_T shift and n_{SS} is also preserved for local fluctuations, as illustrated in Fig. 6(d) for the simplified case where fixed charges are located right at the nanotube-dielectric interface. This linear relationship ensures that the scaling of $\sigma(V_T)$ again approximately follows the trend predicted for conventional bulk silicon FETs—$\sigma(V_T)\propto n_{SS}^{1/2}$ [Fig. 6(a)] and $\sigma(V_T)\propto L_{ch}^{-1/2}$ [Fig. 6(c)] if n_{SS} is high [12,14,39]. However, at more technologically relevant low-n_{SS} values, the variability mainly comes from local fluctuations. In addition, a large fraction of devices is free of any fixed charges near the nanotube. In this scenario, the correlation between V_T shift and the number of nearby fixed charge become more like a step function reflecting the dichotomy between devices that do or do not have any nearby fixed charges, since the V_T shift caused by the first fixed charge is several times larger than that induced by additional ones [Fig. 6(d)]. This nonlinear behavior makes the $\sigma(V_T)$ much larger than in the conventional picture, as shown in Fig. 6(b); and shorter devices actually demonstrate better V_T variability because they have a better chance to be free of any fixed charge in their vicinities as illustrated in Fig. 6(c), a trend opposite to what is described in the conventional Pelgrom picture [39]. For short channel devices built on dielectrics with low n_{SS}, e.g., 20-nm L_{ch} devices made on 10-nm SiO_2 dielectric with a n_{SS} equal to that of the SiO_2-Si interface at 5×10^{10} cm^{-2} [40], most nanotubes are free of nearby fixed charges and thus the $\sigma(V_T)$ could become very small. Yet a few devices still have some fixed charges near the nanotube and demonstrate a unidirectional V_T shift from the average, with the appearance of extreme values up to ~400 mV within ~3000 devices simulated, as shown in Fig. 7(a). In integrated circuits, such large shifts could cause a catastrophic failure of the whole circuit. Indeed, the current design rule for IBM 32-nm technology requires the maximum V_T shift from the average to be below 150 mV. Fortunately, we find that the adoption of a more aggressively

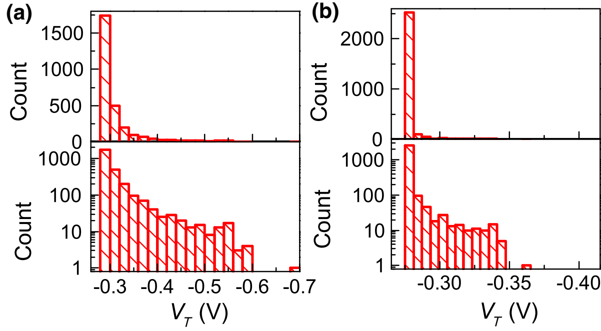

FIG. 7. Histograms showing the V_T distribution of 2800 simulated devices on 10-nm SiO_2 [part (a)] or 2-nm HfO_2 [part (b)] dielectric with a n_{SS} of 5×10^{10} cm^{-2} plotted with the device count in both linear (top frames) and logarithmic (bottom frames) scales.

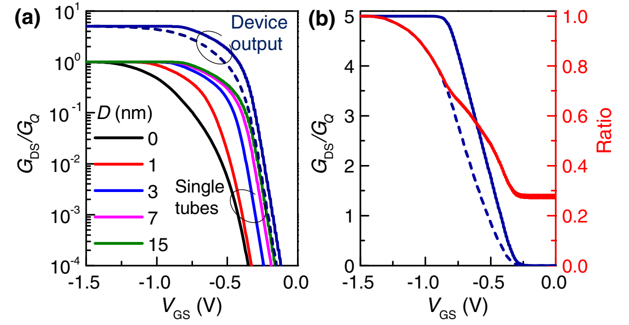

FIG. 8 (a) Device conductance (G_{DS}) normalized with the quantum conductance ($G_Q = 4e^2/h$) as a function of V_{GS} for individual nanotubes with a fixed charge on the oxide surface at 0 (black), 1 (red), 3 (blue), 7 (magenta), and 15 (green) nm away from each of their tube axes projected onto the same surface, as well as multiple tube devices composed of such 5 nanotubes connected in parallel (dashed navy) or 5 nanotubes all without any nearby fixed charge (solid navy). (b) G_{DS}/G_Q as a function of V_{GS} for the multiple tube devices plotted in part (a). The ratio of their output current under identical V_{GS} is illustrated in red with the right axis.

scaled gate dielectric of 2-nm HfO_2 can reduce the V_T shift of even some extreme cases to less than 100 mV, as illustrated in Fig. 7(b). Thus, it is still possible to get the V_T variability performance of FETs built on 1D semiconductors to the level required for very-large-scale integration after some reasonable engineering improvements.

In conventional planar devices, uniformity increases with channel width. While the width of each nanotube is fixed, it is anticipated that practical devices will incorporate several tubes in parallel in each transistor to increase the output power. We find that this actually provides a much greater improvement in uniformity than increasing conventional device width. Figure 8(a) shows the effect on the transfer characteristics from a single positive fixed charge at different distances D from the nanotube, for devices with 100-nm L_{ch} built on 10-nm SiO_2 dielectric. Since nanotubes are 1D semiconductors, connecting multiple nanotubes in parallel will not provide the same averaging effect as a wider channel in the case of planar silicon FETs. Each nanotube will still operate independently, and the overall device output is the sum of current flowing through each nanotube. Then for a hypothetical p-channel device built on these five nanotubes as the multitube channel, the device V_T is determined almost entirely by the single-tube component with the minimal V_T shift, since the device subthreshold current depends exponentially on the difference between V_{GS} and V_T [2,23]. As a result, the device V_T is only shifted by less than 30 mV compared to a "perfect" device built on five nanotubes all free of nearby fixed charges as shown in Fig. 8(a). While this feature provides a great benefit in controlling the uniformity of subthreshold current, in the on state it is not equivalent to making the V_T shift become just 30 mV. The device transconductance in the on state is reduced as each nanotube turns on sequentially. With V_{GS} at -0.5 V above the V_T of the fixed-charge-free device, the on-state conductance of this hypothetic device is over 30% lower, as illustrated in Fig. 8(b); while only 6% reduction is expected for conventional transistors with just a 30-mV shift of V_T. Note that if the polarity for either fixed charges or the device type is reversed compared to the case here, the V_T of a multitube device will be determined by the single tube with the worst V_T shift. However, as discussed above and shown in Fig. 1(c) as well as in the Supplemental Material, Fig. S1(b) [28], in that case the impact on device operation from fixed charges becomes negligible, especially in the regime where n_{SS} is low and the device V_T variability is dominated by local potential fluctuations.

IV. CONCLUSION

In conclusion, we have calculated the effect of randomly distributed fixed charges on the performance of ballistic SWNT FETs using a microscopic model, and achieved good agreement with recent experiments. The device uniformity can be improved with thinner gate oxide, high-κ dielectrics, and better passivation to reduce the trapped charge density, and is correlated with the device dimensions. Because of the 1D nature of the SWNTs and the ballistic transport, the improvement of V_T variability upon scaling these parameters can deviate dramatically from the trend for conventional silicon transistors, even giving an opposite trend with L_{ch} scaling at low surface-charge density. In addition, we find that random fixed charges are a major unrecognized factor limiting the subthreshold swing in SWNT FETs built on scaled gate oxide, as verified by a combination of experiments and simulations. These results provide a better understanding of the unique variability characteristics of ballistic SWNT transistors, and serve as guidelines for future work to improve their uniformity and subthreshold performance, as

well as designing practical large-scale-integrated nanotube circuits.

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