Variability in Carbon Nanotube Transistors: Improving Device-to-Device Consistency

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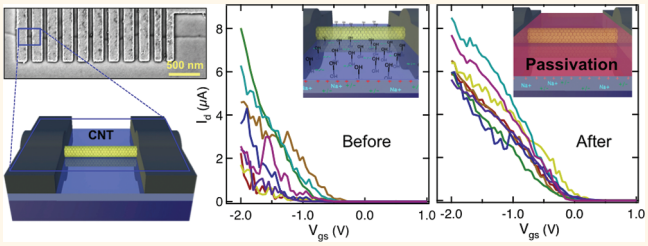
ABSTRACT



The large amount of hysteresis and threshold voltage variation in carbon nanotube transistors impedes their use in highly integrated digital applications. The origin of this variability is elucidated by employing a top-coated, hydrophobic monolayer to passivate bottom-gated devices. Compared to passivating only the supporting substrate, it is found that covering the nanotube channel proves highly effective and robust at improving device-to-device consistency—hysteresis and threshold voltage variation are reduced by an average of 84 and 53%, respectively. The effect of gate and drain—source bias on hysteresis is considered, showing strong dependence that must be accounted for when analyzing the effectiveness of a passivation layer. These results provide both key insight into the origin of variability in carbon nanotube transistors and a promising path for resolving this significant obstacle.

KEYWORDS: hysteresis · carbon nanotube transistors · threshold voltage · CNTFET · variability

With ballistic transport, a unique 1D electronic structure, and ultrathin body (~1 nm), single-walled carbon nanotubes (CNTs) have nearly ideal properties for a channel material in a future transistor technology.[1] The superb low-voltage performance at aggressively scaled channel lengths makes CNT field-effect transistors (CNTFETs) especially suitable for highly integrated digital nanoelectronics.[2] As the processes to separate/purify semiconducting CNTs[3−6] and place them in desired locations on substrates[7−10] continue to progress, it is critical to address the remaining device-level issues of nanotube transistors. Among the remaining challenges is that CNTFETs are plagued by device-to-device variability, including gate hysteresis and imprecise threshold voltage (V_{th}) control. Such variability is largely a result of the entire channel of a CNT being on its surface, yielding a high level of sensitivity to neighboring charges and/or traps. To consider CNTFETs for a future digital technology, the variation in V_{th} and the considerable hysteresis must be substantially reduced or eliminated.

The origin of variation in CNTFETs is a subject of some debate in the literature. One of the earliest reports concluded that water molecules adsorbed on the hydroxylated gate oxide surface—which supports the nanotube—are the cause of hysteresis.[11] Several other studies have corroborated this conclusion,[12−17] including one that used vacuum annealing under different conditions to selectively drive off certain molecules, showing that both water and oxygen adsorbates contribute to the gate variation.[18] In direct contrast to previous reports,[11,18] Lee *et al.* concluded that vacuum annealing has no effect on hysteresis and that the primary cause is from charge transfer between the CNT and charge traps at the silicon oxide/ambient interface (interaction with the surface silanol groups).[19] Still others suggest that the main mechanism is the trapping of carriers within the gate oxide.[20,21] There are also more specific results on the effect of nanotube diameter (larger diameter yields larger hysteresis)[22] and the role of high electric fields on the rearranging of traps near the nanotube.[23]

When considering the breadth of results from previous work, it is important to note the significant impact that different gate configurations can have on the hysteresis and V_{th} variation. Even though most of the reports used similar bottom-gated structures with SiO_2 on doped Si substrates, the

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quality of the SiO_2 will play a critical role in unwanted charge density. Interestingly, the majority of results for reducing the gate variation are from bottom-gated devices, with only a few involving top-gate configurations. The foremost reason for the bottom-gate preference is the ease of fabrication, specifically with a substrate gate. Another reason is the greater diversity of passivation materials that can be used with a bottom-gate configuration. While the most ideal geometry may be a gate-all-around structure, devices implementing such a gate are limited and not optimized.[24,25]

Several methods for reducing gate variation in CNTFETs have been published, with nearly all focusing on the need for surface passivation and generally falling into two categories: (1) coating a bottom-gate dielectric with a molecular monolayer before CNT placement, and (2) depositing oxide on top of CNTs after placement. Note that there are many reports on eliminating hysteresis by using pulsed gate voltage characterization,[18,26,27] but this is merely an experimental technique for understanding the origin of hysteresis rather than a practical solution for digital applications. Approach (1) was demonstrated with hydrophobic self-assembled monolayers (SAMs), which passivate the Si−OH hydroxyl groups on the oxide surface, thus reducing the number of mobile adsorbates that can attach.[13,15,28] This approach is mildly effective at lowering hysteresis but has an inherent downside—adding to the equivalent oxide thickness (EOT) for bottom-gated devices. For approach (2), high-k dielectrics, such as Al_2O_3 or TiO_2, are deposited using atomic layer deposition (ALD) or physical vapor deposition to cover the substrate-supported CNT.[16,29] Elevated temperatures during deposition can help drive off adsorbates, but oxides are not robust barriers for further water/oxygen diffusion in air. Furthermore, the few reports that exist do not provide substantial evidence of hysteresis reduction from the coating.

In this work, the benefits from both of the above-mentioned approaches are combined by coating bottom-gated CNT devices—after nanotube placement—with a hydrophobic SAM in a vacuum environment at elevated temperature. This approach keeps the SAM from adding to the EOT, enables the removal of adsorbates in the heated vacuum deposition environment, provides a robust barrier to further adsorbate diffusion, and passivates the nanotube channel in addition to the surrounding oxide. To determine the magnitude of V_{th} variation, sets of 10 devices were assembled on the same nanotube channel to avoid variation caused by different CNTs. Additionally, hundreds of devices (each on a different nanotube) on the same chip were tested before and after the SAM passivation to determine the efficacy of the treatment at reducing gate variation. The impact of drain−source and gate−source (V_{ds} and V_{gs}) bias on hysteresis was studied, showing a strong dependence on V_{ds} that undermines the usefulness of many previous

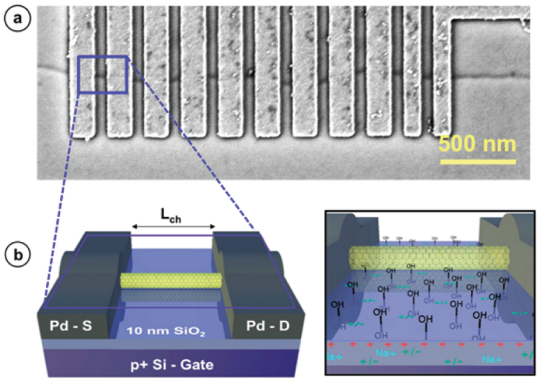

Figure 1. (a) SEM image of 10 CNTFETs assembled on the same nanotube. (b) Schematic of device structure, including 10 nm SiO_2 gate dielectric and Pd source/drain contacts. Higher magnification schematic illustrates the potential sources of variation. The OH group on the hydroxylated oxide surface could also be adsorbed H_2O or O_2, which function as surface mobile charges. The charge traps (green +/−) can be interfacial or within the oxide. The mobile ions (blue Na^+) may be present in samples derived from solution-dispersed CNTs that are wrapped in a Na-containing surfactant. The fixed oxide charge (red +) is from dangling bonds.

reports that only examined hysteresis at low biases. It should be noted that deposition of the SAM from solution phase was also studied and provided barely discernible reduction in hysteresis and V_{th} variation—the gas-phase deposition is critical to the success of this passivation approach owing to the dry vacuum environment and elevated temperature.

RESULTS AND DISCUSSION

***V_{th}* Variation in Devices on the Same CNT.** All of the devices in this work utilized a substrate bottom-gate of p^+ Si with a 10 nm SiO_2 gate dielectric. Sets of up to 10 devices were fabricated on individual chemical vapor deposition (CVD)-grown nanotubes (as shown in Figure 1) to observe the amount of variation present when the channel material and length are consistent. Keeping the same CNT channel is significant because the energy band gap (E_g) is inversely proportional to the nanotube diameter (d_{CNT}); therefore, a change in d_{CNT} will have an effect on the threshold voltage. The transfer curves in Figure 2a are from eight neighboring devices on the same CNT and have V_{th} spanning approximately 0.8 V. This means that charges and traps in the vicinity of the nanotube channels are inhomogeneous enough to cause nearly a 1 V spread in the transfer curves.

Potential origins of the observed variation in Figure 2a are illustrated in the schematic of Figure 1b. Some amount of mobile and fixed oxide charges are to be expected for the relatively thick SiO_2 dielectric (10 nm) used here—note that the dielectric was annealed in forming gas at high temperature to minimize trapped charges. As for mobile charge traps, they can be present both in the oxide and in the form of adsorbed molecules such as water and oxygen on the Si−OH-terminated

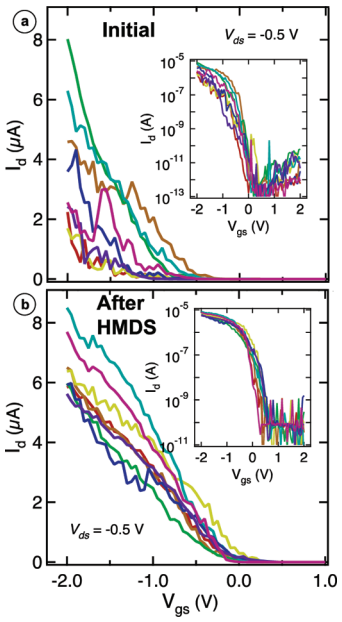

Figure 2. (a) Initial transfer curves from 8 CNTFETs on the same CVD-grown nanotube. (b) Transfer curves from the same devices as in (a), after a 24 h passivation coating of HMDS at 150 °C; the range of V_{th} reduces from ~800 to ~400 mV. All devices have L_{ch} = 80 nm. Insets are of the same data plotted on a log scale to show the subthreshold off-state.

oxide surface by attaching to the silanol groups. It is important to determine how much each of these types of charges is contributing to the observed variation. While many of the charges represented in Figure 1b will vary in density and type based on the gate dielectric chosen, the surface charges and adsorbates will be present in any oxide-CNT device.

As mentioned above, previous reports have reduced the charge traps on the surface by coating the oxide with a hydrophobic SAM prior to nanotube deposition. In this work, instead of applying the SAM prior to the CNT channels, it was coated after the devices were completely fabricated and tested to determine the before and after effect. There are four key aspects to the SAM deposition process used in this study. First, deposition was carried out in the gas phase, in a vacuum environment (Torr range) to aid in desorption of oxygen. Second, the deposition temperature was 150 °C, which further aided in driving off adsorbates (such as water) from the hydroxylated oxide surface. Third, the SAM was deposited both on the oxide (except for the small portion of oxide under the CNT) and over the CNT as evidenced by atomic force microscope (AFM) images taken before and after deposition (see Supporting Information). Coating the CNT is significant because water molecules adsorb not only on the Si−OH-terminated SiO_2 but also on the nanotube itself.[11,13] The fourth important trait of the current SAM deposition process is the use of hydrophobic monolayers, which work as effective diffusion barriers to water and/or oxygen, enabling the devices to be stable in air. Two monolayers were studied: hexamethyldisilazane (HMDS) and octadecyltrichlorosilane (ODTS). The results herein are from HMDS, while the ODTS results are given in the Supporting Information.

The outcome of applying a 24 h gas-phase coating of HMDS to the eight neighboring CNTFETs in Figure 2a is shown in Figure 2b. Passivating the devices with the SAM reduced the range of V_{th} among the devices from 800 mV down to approximately 400 mV. Additionally, the curves were all shifted to the right (more positive V_{th}), denoting that there is a change in doping of the CNT channel, from either reducing the surrounding charges and thus "undoping" or introducing new dopants from the charged molecules of the SAM—most likely a combination of both mechanisms. A 50% reduction in the V_{th} range is substantial, yet the devices still span 400 mV. Therefore, large sets of devices were studied to further elucidate the source of variation.

***V_{th}* Variation in Large Sets of Devices.** Important information was also gleaned from a distribution of devices having nearly the same L_{ch} but different nanotube channels. Hundreds of devices were fabricated on a chip from solution-processed nanotubes randomly dispersed across the surface at a density that nominally yields one CNT per device. Using a semiautomated probe station, semiconducting nanotube devices were identified and tested. To help ensure that the devices consisted of nominally one CNT, a conditional electrical test was used to confirm that the drain current at a given gate bias fell within the range expected for a single nanotube (as determined from previous experiments on similar device structures). Subthreshold curves from such a chip are given in Figure 3a, where the range for V_{th} (1.2 V) is approximately 0.4 V greater than in the devices built along the same CNT. This larger variation is partly impacted by the different d_{CNT} (thus different E_g) among the devices as well as the disparity in channel length—while all devices are designed at 300 nm, the CNTs are in various orientations that affect actual channel length.

Because the charges causing V_{th} variation are inhomogeneous across the substrate (as concluded from Figure 2 data), it is most helpful to consider the distribution of V_{th} from a large number of devices on the same chip. Such a distribution is plotted in Figure 3b, along with the impact that a 1 h HMDS passivation treatment has on the same devices. The 1 h coating only slightly tightens the distribution and shifts V_{th} mildly to the right (more positive). In contrast, coating HMDS in the same process but for 24 h has a sizably different effect, as seen with the before and after distributions in Figure 3c. The considerable difference made by longer HMDS coating time is mainly attributed to more effective desorption of molecular adsorbates due to longer exposure to vacuum and high temperature. An additional factor is that the 1 h treatment does not likely provide a complete

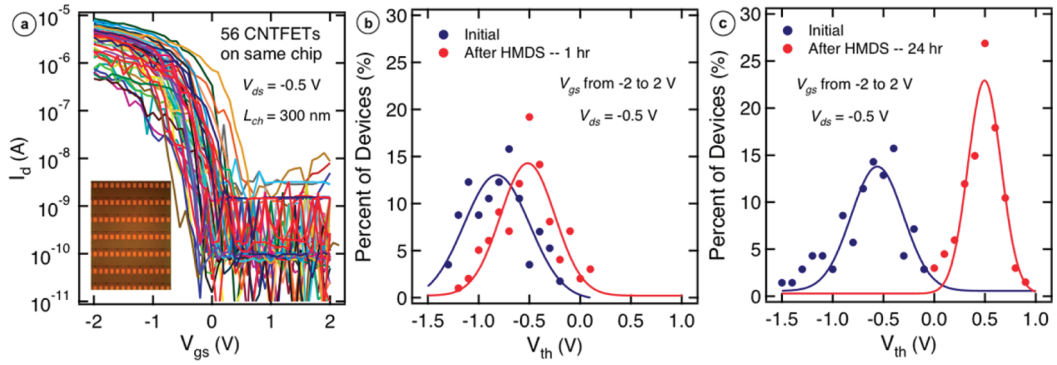

Figure 3. (a) Subthreshold characteristics from 56 CNTFETs on the same chip (each on a different nanotube), with each device designed at L_{ch} = 300 nm. The CNTs are laser ablation synthesized and dispersed onto the SiO_2 from solution (inset shows optical image of several rows of the type of contacts used to test the devices). (b) Distribution of threshold voltage for the 56 CNTFETs on the same chip before (initial) and after passivation with HMDS that was coated for 1 h. The solid lines are Gaussian fits to the data, with standard deviations of 0.31 and 0.26 V for the initial and after HMDS data, respectively. (c) Similar distribution for 52 devices on a chip passivated with HMDS that was coated for 24 h. Standard deviations for the Gaussian fits are 0.27 and 0.16 V for the initial and after HMDS data, respectively. In all cases, V_{th} was extracted by linear fit to the transfer curve (swept from negative V_{gs} to positive V_{gs}) at −0.5 V drain bias.

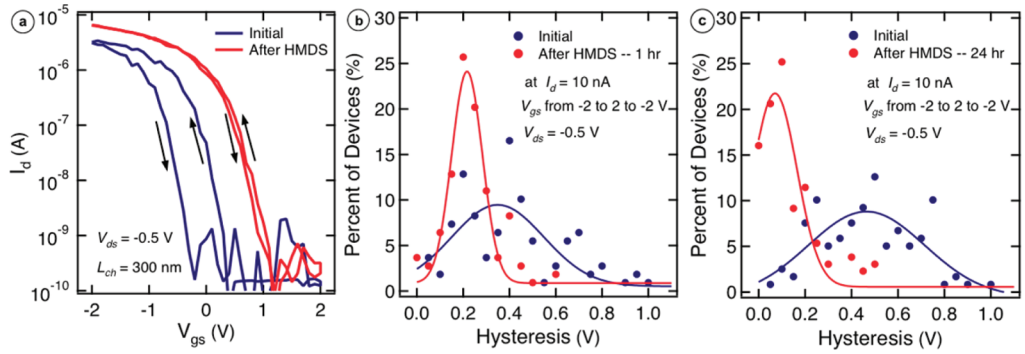

Figure 4. (a) Subthreshold characteristics from a single device showing nearly complete elimination of hysteresis after 24 h HMDS passivation. (b) Distribution of hysteresis for 56 CNTFETs on the same chip before (initial) and after passivation with HMDS that was coated for 1 h. The solid lines are Gaussian fits to the data, with standard deviations of 0.20 and 0.07 V for the initial and after HMDS data, respectively. (c) Similar distribution for 52 devices on a chip passivated with HMDS, coated for 24 h. Standard deviations for the Gaussian fits are 0.24 and 0.08 V for the initial and after HMDS data, respectively. In all cases, hysteresis was extracted from the subthreshold curve at −0.5 V drain bias and 10 nA of drain current.

monolayer of HMDS. The 24 h coating, however, forms a complete monolayer that passivates all devices. This difference in coating uniformity was confirmed by the contact angle of water measured on the samples after HMDS deposition. For the 1 h coating, the contact angle was 65° *versus* 77° from the 24 h coating—higher contact angle signifies higher hydrophobicity and thus a more complete monolayer.

Another important consideration when determining the magnitude of V_{th} variation in a set of devices is the direction that V_{gs} is swept. For all of the results herein, V_{gs} was swept from the *on*-state (negative voltage) to the off-state (positive voltage) when extracting V_{th}. If the range of V_{th} were examined for the devices by sweeping them in the opposite fashion, then there is an impact that can be seen when comparing a small number of devices (hysteresis differences among the devices is the cause of this difference). However, when examining the V_{th} distribution from a large set of devices, as in Figure 3, the sweep direction of V_{gs} does not noticeably affect the range of V_{th}.

Hysteresis Reduction in Large Sets of Devices. Gate hysteresis is another deleterious effect of unwanted charges in CNTFETs, as shown in the subthreshold curves of Figure 4a. Mobile charge traps, which rearrange under the influence of certain gate bias and/or source−drain electric field conditions, cause hysteretic behavior in the characteristics. Passivation with the 24 h top coating of HMDS proves remarkably effective at removing hysteresis (average hysteresis from 52 devices reduced from 0.5 to 0.08 V), as seen in the Figure 4a device and the distributions from many devices on the same chip in Figure 4c. As with the reduction in threshold voltage variation, the 1 h coating of HMDS was only marginally effective at lessening hysteresis.

The ability of the top-coated HMDS monolayer to so dramatically reduce hysteresis provides some important information regarding the root causes of such variation. First of all, the passivation process focuses

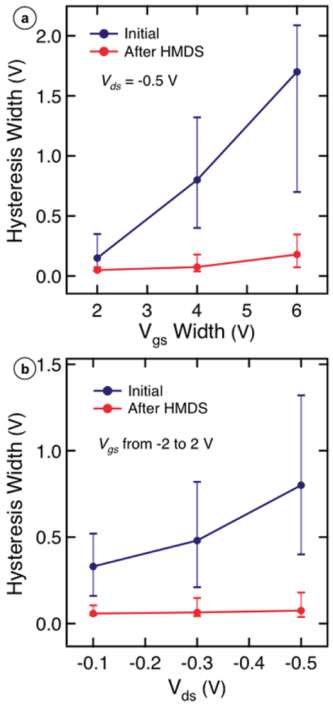

Figure 5. Voltage dependence of hysteresis from a large set of devices. (a) Dependence of hysteresis on gate voltage sweep range before and after 24 h HMDS passivation on a chip with 52 CNTFETs. The three V_{gs} widths tested were -1 V $\leq V_{gs} \leq 1$ V, -2 V $\leq V_{gs} \leq 2$ V, and -3 V $\leq V_{gs} \leq 3$ V. (b) Dependence of hysteresis on drain bias for the same chip as in (a). For all devices, hysteresis was extracted at a drain current of 10 nA. The data points in (b) and (c) are the average from all devices, and the error bars indicate the high and low points.

specifically on reducing unwanted surface charges—adsorbates on the Si–OH groups and interface trap charges. Therefore, the nearly complete elimination of hysteresis for most of the devices suggests that it was indeed these surface charge traps that are primarily responsible for hysteretic behavior. As for the small percentage of devices that still show hysteresis, they could either be affected by local trapped charge in the oxide, defects in the nanotubes acting as charge centers, or still incomplete coverage with the HMDS.

Voltage Dependence of Hysteresis. Hysteresis is a difficult effect to compare from different studies because it is highly sensitive to the voltage bias conditions and gate geometry. Surprisingly, despite the well-known sensitivity of hysteresis to gate and drain–source biases, no previous studies have considered this important dependence in their reports on CNTFET hysteresis. Furthermore, all previous studies to our knowledge primarily explored hysteresis at $|V_{ds}| \leq 0.2$ V, which provides a dramatically lower hysteresis than observed at more technologically relevant bias conditions. Here we carefully considered the bias dependence of hysteresis in the devices before and after SAM passivation, as shown in Figure 5a,b. Note the strong dependences of hysteresis on the gate sweep width, particularly before passivation. As the width of the gate sweep increases, more mobile charges are activated and hysteresis increases (this could also be impacted by increased charge injection from the gate into the oxide due to the higher electric field). For V_{ds}, the increased source–drain field also activates stray charges that contribute to the hysteresis. There remains a significant dependence of hysteresis on V_{ds} even after passivation. For the hysteresis distribution data in Figure 4b,c, a gate sweep width of 4 V was used (-2 V $\leq V_{gs} \leq 2$ V) at $V_{ds} = -0.5$ V.

Origin of Variation in CNTFETs. Reduction of V_{th} variation and hysteresis by top-coated surface passivation is evidence of the sizable contribution of surface charges. While the remaining variation in the Figure 3c V_{th} distribution could be partially attributed to CNT channel differences, the Figure 2b devices on the same CNT still show ~400 mV of variation after SAM passivation. Considering the effectiveness of the hydrophobic SAM in suppressing hysteresis, this remaining variation in V_{th} is attributed to fixed and trapped charges within the oxide. By thinning the oxide and improving the annealing and other treatments, these remaining charges should be able to be reduced and, subsequently, the uniformity of V_{th} should improve. Conclusive from this study is that a gas-phase top coating of a hydrophobic SAM (covering both the dielectric and CNT) is the most effective process for reducing variability in CNTFETs presented to date.

CONCLUSIONS

By studying sets of devices on the same nanotube, as well as large distributions of CNTFETs on the same chip, critical information regarding the origin of V_{th} variation and hysteresis was obtained. Passivation of the oxide and CNT with a hydrophobic monolayer proved highly effective at reducing V_{th} variation and quenching hysteresis. For the first time, the effect of gate and drain–source bias conditions on hysteresis was considered, showing strong dependence that must be accounted for when analyzing the effectiveness of a passivation process. This study shows promise for an optimized passivation layer and gate dielectric to be able to eliminate the substantial variation present in these molecular-channel devices.

METHODS

Synthesis and Transfer of Long CNTs for Devices on Same Nanotube. Single-walled CNTs were synthesized on ST-cut single-crystal quartz substrates (Hoffman Inc.). The substrates were first thermally annealed at 900 °C for 9 h. Iron catalyst stripes consisting of thin films (2–3 Å) were deposited by electron-beam evaporation and patterned by photolithography (ASML PAS 5500/60 i-line Stepper) and lift-off. Next, the substrates

were annealed in air at 550 °C for 1 h, followed by chemical vapor deposition (CVD) growth of aligned CNTs between the catalyst islands with CH_4 (1000 sccm) and H_2 (120 sccm) as the feeding gases at 865 °C. After synthesis, the CNTs were coated with 150 nm Au and transferred onto p+ Si substrates that had 10 nm thermal SiO_2 that had been annealed in forming gas (95% Ar/5% H_2) at 450 °C for 30 min. The transfer process is outlined in detail in previous publications.[30,31]

Fabrication of Ten Devices along the Same CNT. Following transfer, electron-beam lithography (EBL) was used to pattern source/drain contacts with 3 μm channel lengths for hundreds of devices on a chip into the PMMA resist. Contact metal of 0.2 nm Ti/20 nm Pd/30 nm Au was then electron-beam evaporated followed by lift-off in 80 °C acetone. An additional EBL step was used to isolate the nanotube channels to an active device region of 1 μm width by protecting them with PMMA while the exposed CNTs were removed using oxygen plasma etching. Using a Cascade Summit semiautomated probe station, 3 μm long semiconducting nanotubes were located and an additional EBL step was carried out to fabricate a set of 10 CNTFETs along the 3 μm nanotube. The devices were electrically tested in air with no further treatment.

Fabrication of Hundreds of Devices on a Chip. To obtain the distributions data, CNTs synthesized by arc-discharge (Hanwha Nanotech) were mixed with a stock solution of 1% w/v of sodium cholate. The mixture was sonicated for 30 min with a higher power horn sonicator (600 W, 20% amplitude, 20 kHz). The solution was then centrifuged at 10 000 rpm for 1 h (Beckman Coulter, Optima L-100 XP ultracentrifuge). After centrifugation, the supernatant was collected and then used to fill a centrifuge tube halfway. A 30% Iodixinol (Sigma Aldrich) solution with 1% sodium cholate was then layered below the CNT solution to be used as a stop layer. A second centrifugation step was then performed at 41 000 rpm for 18 h. The stop layer produced a narrow band of purified CNTs near the middle of the tube, which was collected with a glass pipet. This dense solution was dialyzed in 1% sodium cholate solution where the solution was changed two times over 48 h. The highly concentrated, purified CNT solution was then diluted (1:100 by volume) with 1% w/v sodium cholate solution. The CNTs were then drop-cast onto p+ Si substrates that had 10 nm thermal SiO_2 that had been annealed in forming gas (95% Ar/5% H_2) at 450 °C for 30 min. EBL was used to pattern electrodes 15 μm wide with 300 nm channel lengths, yielding approximately 0−3 CNTs per device. The hundreds of devices were then tested on a semiautomated probe station in air with no further treatment.

Passivation with HMDS or ODTS. After performing initial characterization of the devices, the chips were placed in a glass desiccator filled with desiccant along with a 2 mL solution of HMDS (Sigma Aldrich) or ODTS (Sigma Aldrich) in an open glass vial. The desiccator was then evacuated using house vacuum. The sealed desiccator was then put in an oven at 150 °C and kept for the desired deposition time. After deposition, the samples were cooled and the devices were retested in air.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Additional experimental details. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Appenzeller, J. Carbon Nanotubes for High-Performance Electronics—Progress and Prospect. *Proc. IEEE* **2008**, *96*, 201–211.
2. Franklin, A. D.; Chen, Z. Length Scaling of Carbon Nanotube Transistors. *Nat. Nanotechnol.* **2010**, *5*, 858–862.
3. Liu, J.; Hersam, M. C. Recent Developments in Carbon Nanotube Sorting and Selective Growth. *MRS Bull.* **2010**, *35*, 315–322.
4. Hersam, M. C. Progress towards Monodisperse Single-Walled Carbon Nanotubes. *Nat. Nanotechnol.* **2008**, *3*, 387–394.
5. Antaris, A. L.; Seo, J.-W. T.; Green, A. A; Hersam, M. C. Sorting Single-Walled Carbon Nanotubes by Electronic Type Using Nonionic, Biocompatible Block Copolymers. *ACS Nano* **2010**, *4*, 4725–4732.
6. Stürzl, N.; Hennrich, F.; Lebedkin, S.; Kappes, M. M. Near Monochiral Single-Walled Carbon Nanotube Dispersions in Organic Solvents. *J. Phys. Chem. C* **2009**, *113*, 14628–14632.
7. Vijayaraghavan, A.; Hennrich, F.; Stürzl, N.; Engel, M.; Ganzhorn, M.; Oron-Carl, M.; Marquardt, C. W.; Dehm, S.; Lebedkin, S.; Kappes, M. M.; *et al.* Toward Single-Chirality Carbon Nanotube Device Arrays. *ACS Nano* **2010**, *4*, 2748–2754.
8. Bardecker, J. A.; Afzali, A.; Tulevski, G. S.; Graham, T.; Hannon, J. B.; Jen, A. K.-Y. Directed Assembly of Single-Walled Carbon Nanotubes *via* Drop-Casting onto a UV-Patterned Photosensitive Monolayer. *J. Am. Chem. Soc.* **2008**, *130*, 7226–7227.
9. Sarker, B. K.; Shekhar, S.; Khondaker, S. I. Semiconducting Enriched Carbon Nanotube Aligned Arrays of Tunable Density and Their Electrical Transport Properties. *ACS Nano* **2011**, *5*, 6297–6305.
10. Shekhar, S.; Stokes, P.; Khondaker, S. I. Ultrahigh Density Alignment of Carbon Nanotube Arrays by Dielectrophoresis. *ACS Nano* **2011**, *5*, 1739–1746.
11. Kim, W.; Javey, A.; Vermesh, O.; Wang, Q.; Li, Y.; Dai, H. Hysteresis Caused by Water Molecules in Carbon Nanotube Field-Effect Transistors. *Nano Lett.* **2003**, *3*, 193–198.
12. Ong, H. G.; Cheah, J. W.; Zou, X.; Li, B.; Cao, X. H.; Tantang, H.; Li, L.-J.; Zhang, H.; Han, G. C.; Wang, J. Origin of Hysteresis in the Transfer Characteristic of Carbon Nanotube Field Effect Transistor. *J. Phys. D: Appl. Phys.* **2011**, *44*, 285301.
13. McGill, S. A.; Rao, S. G.; Manandhar, P.; Xiong, P.; Hong, S. High-Performance, Hysteresis-Free Carbon Nanotube Field-Effect Transistors *via* Directed Assembly. *Appl. Phys. Lett.* **2006**, *89*, 163123.
14. Mattmann, M.; Roman, C.; Helbling, T.; Bechstein, D.; Durrer, L.; Pohle, R.; Fleischer, M.; Hierold, C. Pulsed Gate Sweep Strategies for Hysteresis Reduction in Carbon Nanotube Transistors for Low Concentration NO_2 Gas Detection. *Nanotechnology* **2010**, *21*, 185501.
15. Hu, P.; Zhang, C.; Fasoli, A; Scardaci, V.; Pisana, S.; Hasan, T.; Robertson, J.; Milne, W.; Ferrari, A. Hysteresis Suppression in Self-Assembled Single-Wall Nanotube Field Effect Transistors. *Physica E* **2008**, *40*, 2278–2282.
16. Helbling, T.; Hierold, C.; Roman, C.; Durrer, L.; Mattmann, M.; Bright, V. M. Long Term Investigations of Carbon Nanotube Transistors Encapsulated by Atomic-Layer-Deposited Al_2O_3 for Sensor Applications. *Nanotechnology* **2009**, *20*, 434010.
17. Rinkiö, M.; Zavodchikova, M. Y.; Törmä, P.; Johansson, A. Effect of Humidity on the Hysteresis of Single Walled Carbon Nanotube Field-Effect Transistors. *Phys. Status Solidi B* **2008**, *245*, 2315–2318.
18. Lin, H.; Tiwari, S. Localized Charge Trapping Due to Adsorption in Nanotube Field-Effect Transistor and Its Field-Mediated Transport. *Appl. Phys. Lett.* **2006**, *89*, 073507.
19. Lee, J. S.; Ryu, S.; Yoo, K.; Choi, I. S.; Yun, W. S.; Kim, J. Origin of Gate Hysteresis in Carbon Nanotube Field-Effect Transistors. *J. Phys. Chem. C* **2007**, *111*, 12504–12507.
20. Robert-Peillard, A.; Rotkin, S. V. Modeling Hysteresis Phenomena in Nanotube Field-Effect Transistors. *IEEE Trans. Nanotechnol.* **2005**, *4*, 284–288.
21. Vijayaraghavan, A.; Kar, S.; Soldano, C.; Talapatra, S.; Nalamasu, O.; Ajayan, P. M. Charge-Injection-Induced Dynamic Screening and Origin of Hysteresis in Field-Modulated Transport in Single-Wall Carbon Nanotubes. *Appl. Phys. Lett.* **2006**, *89*, 162108.

22. Pop, E.; Dutta, S.; Estrada, D.; Liao, A. Avalanche, Joule Breakdown and Hysteresis in Carbon Nanotube Transistors. *IEEE Int. Reliab. Phys. Symp. Proc.* **2009**, 405–408.
23. Fuhrer, M. S.; Kim, B. M.; Dürkop, T.; Brintlinger, T. High-Mobility Nanotube Transistor Memory. *Nano Lett.* **2002**, *2*, 755–759.
24. Franklin, A. D.; Sayer, R. A.; Sands, T. D.; Fisher, T. S.; Janes, D. B. Toward Surround Gates on Vertical Single-Walled Carbon Nanotube Devices. *J. Vac. Sci. Technol., B* **2009**, *27*, 821–826.
25. Chen, Z. H.; Farmer, D.; Xu, S.; Gordon, R.; Avouris, P.; Appenzeller, J. Externally Assembled Gate-All-Around Carbon Nanotube Field-Effect Transistor. *IEEE Electron Device Lett.* **2008**, *29*, 183–185.
26. Estrada, D.; Dutta, S.; Liao, A.; Pop, E. Reduction of Hysteresis for Carbon Nanotube Mobility Measurements Using Pulsed Characterization. *Nanotechnology* **2010**, *21*, 85702.
27. Mattmann, M.; Bechstein, D.; Roman, C.; Chikkadi, K.; Hierold, C. Reduction of Gate Hysteresis above Ambient Temperature *via* Ambipolar Pulsed Gate Sweeps in Carbon Nanotube Field Effect Transistors for Sensor Applications. *Appl. Phys. Lett.* **2010**, *97*, 153103.
28. Hur, S.-H.; Yoon, M.-H.; Gaur, A.; Shim, M.; Facchetti, A.; Marks, T. J.; Rogers, J. A. Organic Nanodielectrics for Low Voltage Carbon Nanotube Thin Film Transistors and Complementary Logic Gates. *J. Am. Chem. Soc.* **2005**, *127*, 13808–13809.
29. Kim, S. K.; Xuan, Y.; Ye, P. D.; Mohammadi, S.; Back, J. H.; Shim, M. Atomic Layer Deposited Al_2O_3 for Gate Dielectric and Passivation Layer of Single-Walled Carbon Nanotube Transistors. *Appl. Phys. Lett.* **2007**, *90*, 163108.
30. Patil, N.; Lin, A.; Myers, E. R.; Ryu, K.; Badmaev, A.; Zhou, C.; Wong, H.-S. P.; Mitra, S. Wafer-Scale Growth and Transfer of Aligned Single-Walled Carbon Nanotubes. *IEEE Trans. Nanotechnol.* **2009**, *8*, 498–504.
31. Ryu, K.; Badmaev, A.; Wang, C.; Lin, A.; Patil, N.; Gomez, L.; Kumar, A.; Mitra, S.; Wong, H.-S. P.; Zhou, C. CMOS-Analogous Wafer-Scale Nanotube-on-Insulator Approach for Submicrometer Devices and Integrated Circuits Using Aligned Nanotubes. *Nano Lett.* **2009**, *9*, 189–197.