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Arrays of single-walled carbon nanotubes with full surface coverage for high-performance electronics

Qing Cao*, Shu-jen Han, George S. Tulevski, Yu Zhu, Darsen D. Lu and Wilfried Haensch

Single-walled carbon nanotubes have exceptional electronic properties and have been proposed as a replacement for silicon in applications such as low-cost thin-film transistors and high-performance logic devices[1]. However, practical devices will require dense, aligned arrays of electronically pure nanotubes to optimize performance, maximize device packing density and provide sufficient drive current (or power output) for each transistor[2]. Here, we show that aligned arrays of semiconducting carbon nanotubes can be assembled using the Langmuir–Schaefer method. The arrays have a semiconducting nanotube purity of 99% and can fully cover a surface with a nanotube density of more than 500 tubes/μm. The nanotube pitch is self-limited by the diameter of the nanotube plus the van der Waals separation, and the intrinsic mobility of the nanotubes is preserved after array assembly. Transistors fabricated using this approach exhibit significant device performance characteristics with a drive current density of more than 120 μA μm^{-1}, transconductance greater than 40 μS μm^{-1} and on/off ratios of ~1 × 10^3.

Dense, aligned arrays of carbon nanotubes have previously been created through the chemical vapour deposition (CVD) growth of nanotubes on crystalline substrates[3]. However, this approach creates a mixture of metallic and semiconducting nanotubes, and removing the metallic nanotubes without degrading the performance of the semiconducting ones remains a significant challenge. Alternatively, nanotubes can first be separated in solution[4], and then assembled into aligned arrays under the guidance of an external electric field[5] or a shear force[6,7]. However, with either approach, the highest tube density reported so far is less than 50 tubes/μm (or 10% surface coverage)[8], and such densities are too low to provide the necessary current output to compete with silicon-based devices.

Langmuir–Blodgett and Langmuir–Schaefer techniques are versatile methods for the fabrication of dense arrays of one-dimensional nanomaterials such as single-walled carbon nanotubes[9] or nanowires[10]. The techniques are also scalable and could potentially be used to fabricate arrays on whole wafers.

Figure 1a illustrates our Langmuir–Schaefer-based method for assembling semiconducting single-walled carbon nanotubes into aligned arrays with full surface coverage. Concentrated 99% purity semiconducting nanotubes in 1,2-dichloroethane (DCE) solution are dispersed on the water sub-phase, and spread out to cover the whole surface as a result of the surface tension. Evaporation of the volatile organic solvent makes the nanotubes float on the two-dimensional air/water interface, forming an isotropic phase. Mobile barrier bars are used to apply a uniaxial compressive force that assembles the nanotubes into well-ordered arrays, which represent the two-dimensional smectic phase of liquid-crystal materials. The compression process is stopped when the nanotube film is about to crack, which can be determined from the surface pressure isotherm curve. Parallel nanotube arrays can then be horizontally transferred using the Langmuir–Schaefer method onto various receiving substrates including plastics. Compared with the vertical transfer method (the Langmuir–Blodgett method), the Langmuir–Schaefer method produces films with better alignment and higher yield because of the reduced disturbance of the rigid nanotube Langmuir film on water[11].

Figure 1b presents a scanning electron microscopy (SEM) image of a carbon nanotube film transferred onto a SiO_2/silicon substrate. Closely packed arrays of nanotubes aligned perpendicular to the direction of movement of the bar appear uniformly over a large area. The zoomed-in atomic force microscopy (AFM) image shown in Fig. 1c illustrates the high degree of alignment and linearity of the nanotubes. As nanotube pitch separation may be less than the lateral resolution of the AFM, a more accurate estimation of nanotube density was obtained by placing the aligned arrays onto a silicon nitride membrane window grid for top-view transmission electron microscopy (TEM) imaging (Fig. 1d). This shows that there is full surface coverage, with misalignment defects mainly caused by impurity particles and nanotube loops formed during the assembly process (Supplementary Fig. S1). The high tube density represents a significant improvement over previous results. A cross-sectional TEM image (Fig. 1d, inset; Supplementary Fig. S2) further reveals that the single-walled carbon nanotubes are packed into a uniform double layer across the substrate, with their pitch size self-limited by the nanotube diameter (average, ~1.4 nm; Supplementary Fig. S3) plus the van der Waals separation (~0.4 nm), leading to an estimated tube density as high as 1,100 tubes/μm.

Because nanotubes are not amphiphilic molecules, their most preferred configuration at the air/water interface may not be monolayer, especially given the strong inter-nanotube π–π attractive forces. On the other hand, the nanotube solution, after being dispersed onto the water sub-phase surface, spreads very rapidly over the whole surface driven by the strong surface tension force, which does not favour the formation of aggregates. The intricate balance of (i) the hydrophilic–hydrophobic interactions between nanotubes and water, (ii) the π–π attractive forces between nanotubes, and (iii) the surface tension force at the water sub-phase surface probably leads to the formation of a most favoured bilayer structure of final nanotube Langmuir films. It is possible to break this balance by introducing spacers or repulsive functional groups around the nanotubes and thereby realize a single-layered structure. Although a double layer of semiconducting nanotubes provides twice as many nanotubes as a single layer in the device channel, the device will offer similar performance when integrated into a planar field-effect transistor, even with the scaled device geometry as predicted by a theoretical model (Supplementary Fig. S4). This is because the applied gate electric field can pass through both layers when the tubes are in the off state, as little charge is present in the semiconducting nanotubes when the Fermi level is biased into the middle of the nanotube bandgap. When the device is in

IBM T. J. Watson Research Centre, Yorktown Heights, New York 10598, USA. *e-mail: qcao@us.ibm.com

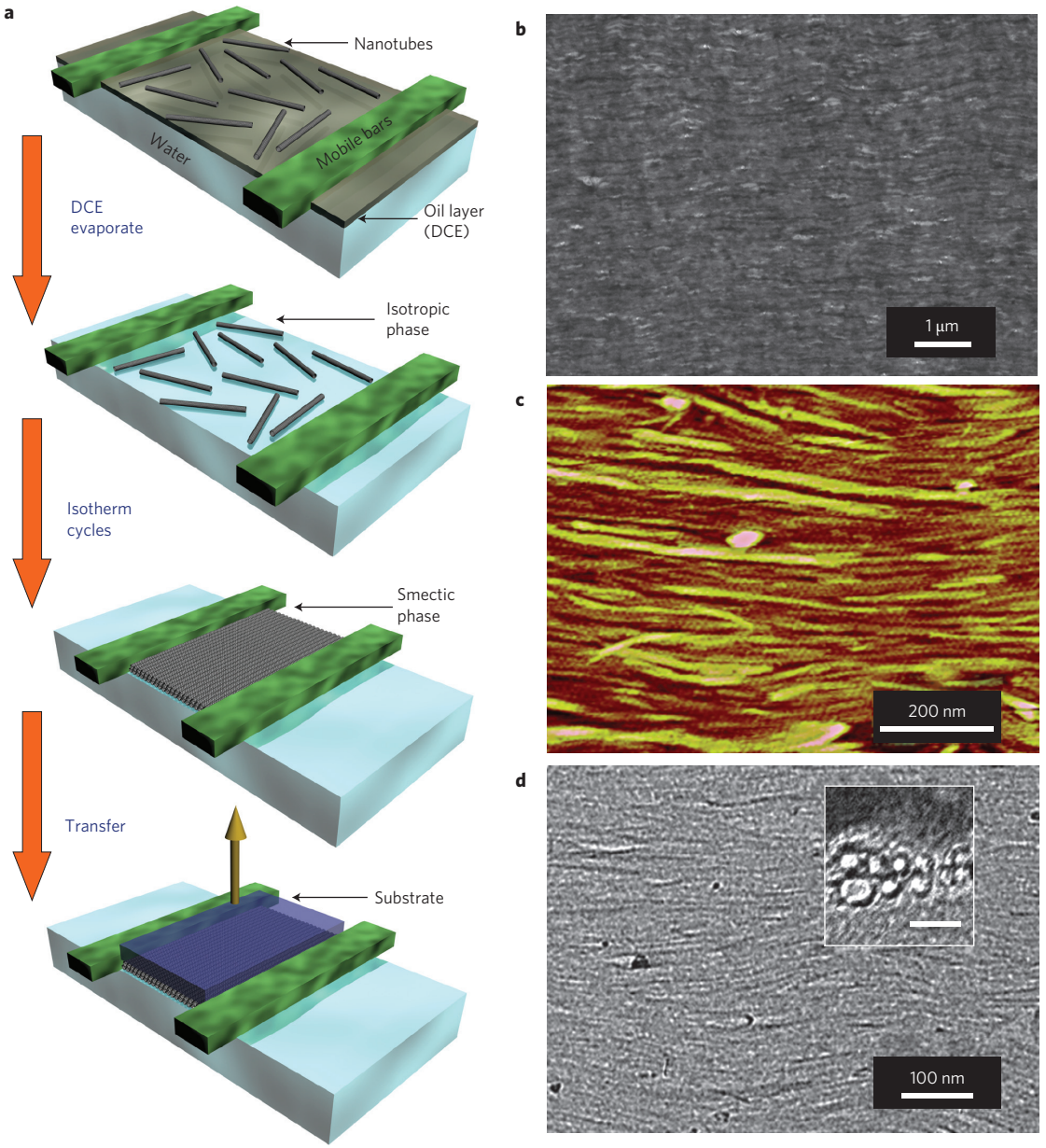

Figure 1 | Assembly and microscopic characterizations of full-coverage aligned arrays of semiconducting single-walled carbon nanotubes. a, Schematic illustration of the Langmuir–Schaefer assembly process. **b–d**, SEM (**b**), AFM (**c**) and top-view TEM (**d**) images of aligned nanotube arrays transferred onto solid substrates. Inset to **d**: high-resolution cross-sectional TEM image (scale bar, 5 nm).

the on state, the electric field will be shielded by the layer closer to the gate electrode. However, the metallic nanotube impurities present in both layers will contribute to current transport.

The alignment and uniformity of the carbon nanotube arrays were characterized in a semi-quantitative fashion by polarized Raman spectroscopy. Figure 2a plots the representative Raman spectra of the tangential G-mode of a nanotube array for various angles α between the polarization direction of the incident laser and the direction of alignment of the nanotubes. The inset to Fig. 2a shows the dependence of the polarized Raman peak intensity on orientation, which is described approximately by a $\cos^2\alpha$ function. Nanotubes with their tube axes parallel to the polarization direction of the laser are more likely to be excited, so measurement of Raman intensity for $\alpha = 0^\circ$ and $\alpha = 90^\circ$ could serve as an indication of the density of aligned and misaligned nanotubes, respectively. The high degree of optical anisotropy with a signal peak-to-valley ratio around 10 indicates the excellent alignment of the nanotube arrays, with most nanotubes aligned within $\pm 17^\circ$ of one another (Supplementary Fig. S5). Figure 2b illustrates the spatial distribution of the normalized G-band intensity measured with $\alpha = 0^\circ$, while Fig. 2c shows the intensity distribution of the G-band acquired with $\alpha = 0^\circ$ ($\parallel$) or $\alpha = 90^\circ$ ($\perp$). These results suggest that the tube density and alignment are quite uniform across the entire substrate, with a standard deviation of less than 15%. Such uniformity in nanotube density does not support the existence of nanotube islands within such arrays with other than bilayer coverage. Further improvements in uniformity and alignment can be achieved by using materials with higher purity and a better controlled experimental environment to minimize the presence of particle defects, together with optimized isothermal cycles during assembly to reduce nanotube looping and curving defects.

Finally, the electronic purity of the deposited carbon nanotube arrays was characterized based on absorption spectra, as shown in Fig. 2d. In the curve for the sample prepared from a 99% pure

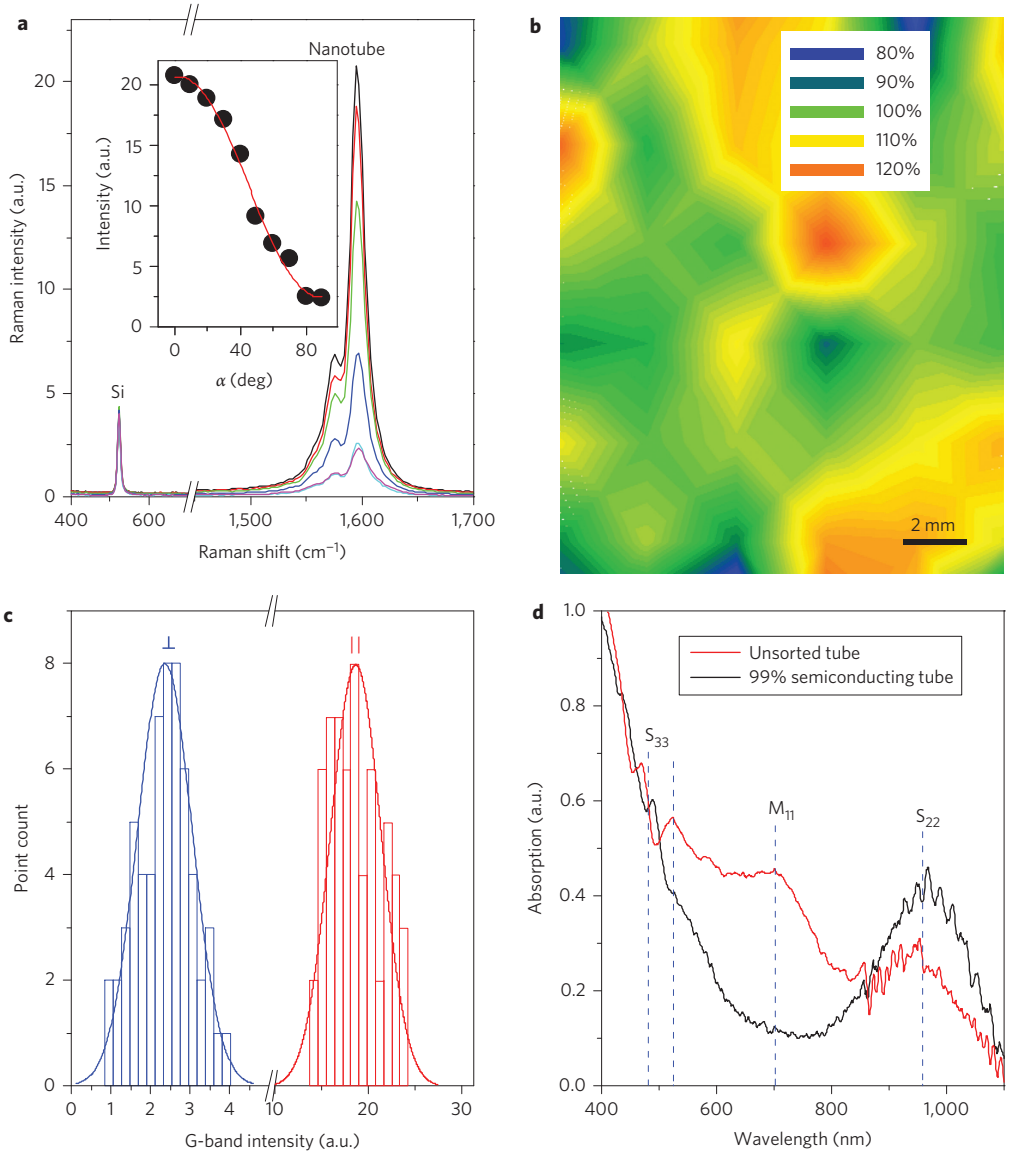

Figure 2 | Optical spectroscopic characterization of full-coverage aligned arrays of semiconducting nanotubes. a, Raman spectra of transverse optical phonon band of crystalline silicon and the tangential G-band of semiconducting nanotube arrays for various angles α (0°, black; 20°, red; 40°, green; 60°, blue; 80°, cyan; 90°, magenta, from top to bottom) between the direction of polarization of the incident 532 nm laser and the overall alignment direction of the nanotubes. Inset: angular dependence of the Raman intensity at 1,594 cm^{-1}. The red solid line represents a fitting to $\cos^2\alpha$ form. **b**, Normalized spatial distribution of the G-band intensity measured with the laser beam polarized along the nanotube alignment direction. **c**, Statistical distribution of G-band intensity measured with the laser beam polarized parallel with (||, red) or perpendicular to (⊥, blue) the direction of nanotube alignment. **d**, Visible/near-infrared absorption spectra of carbon nanotube arrays composed of unsorted nanotubes (red) and 99% semiconducting nanotubes (black) transferred onto a glass substrate. Dashed blue lines mark the positions of transitions characteristic of semiconducting (S_{22} and S_{33}) or metallic (M_{11}) nanotubes.

semiconducting carbon nanotube solution, only transitions associated with semiconducting nanotubes can be observed, which indicates that the electronic purity of the nanotubes is preserved after the suspension and Langmuir–Schaefer assembly processes.

The electrical properties of semiconducting carbon nanotube arrays are evaluated from their integration into both long-channel transistors operating in the percolative regime and short-channel transistors operating in the direct transport regime. For devices with channel length L_{Ch} longer than the average tube length, electrons must travel through several different nanotubes to percolate along the channel, and the highly resistive tube–tube junctions limit this electron transport or effective device mobility μ_{eff}. Such devices are useful in cost-sensitive applications such as moderate-performance thin-film transistors for flexible electronics[12,13]. Most carbon nanotube thin-film transistors reported so far have been constructed with a sub-monolayer of nanotubes with tube densities in the range ~6–10 tubes/μm. Although such low-density nanotube films demonstrate rather respectable μ_{eff} values and on/off ratios[12–16], the very limited surface coverage leads to much lower gate capacitance per unit area (C_i) compared with devices with identical geometry but built on conventional thin-film materials such as amorphous silicon or organic semiconductors. This C_i degradation becomes especially severe with scaled dielectric thickness t_{ox}. Electrostatic modelling suggests that the C_i of a 10 tubes/μm nanotube array is 10 times smaller than that of a film with full surface coverage for $t_{ox} = 5$ nm (Supplementary Fig. S6)[17]. The low C_i will greatly offset the benefit of the higher μ_{eff} obtained with nanotube thin films, leading to both lower-than-expected drive current density under a given bias condition and slower operating speed with a more pronounced effect from parasitic capacitance.

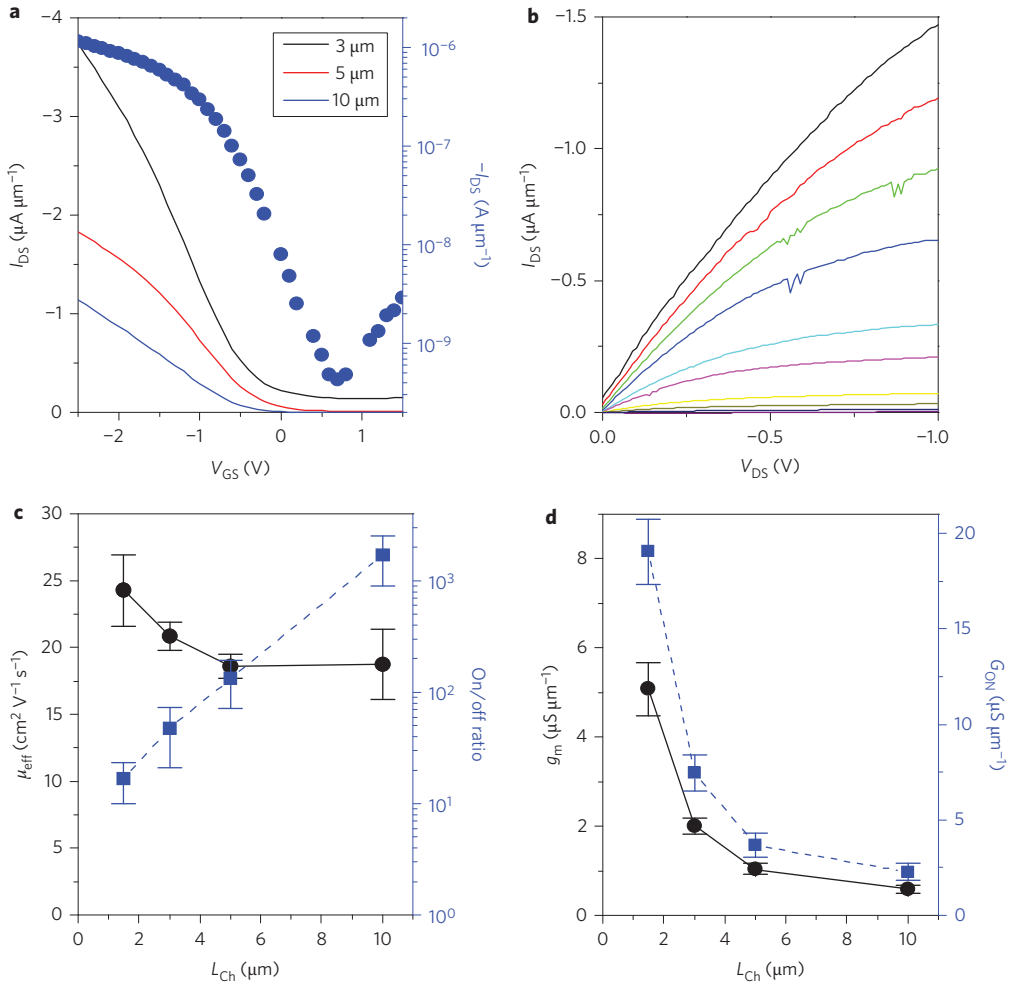

Figure 3 | Electrical properties of thin-film transistors that use 99% purity full-coverage semiconducting nanotube arrays with scaled gate dielectric. **a**, Transfer characteristics in a linear scale (left axis, solid lines) of nanotube thin-film transistors, with channel widths of 10 μm and L_{Ch} of 3 μm, 5 μm and 10 μm, and in a logarithmic scale (right axis, blue dots) for the device with $L_{Ch} = 10$ μm. Applied $V_{DS} = -0.5$ V. **b**, Current–voltage characteristic of a nanotube thin-film transistor with $L_{Ch} = 10$ μm. Applied V_{GS} changes from −1.75 V to 0.5 V with a step of 0.25 V from top to bottom. **c**, μ_{eff} (black circles and solid line, left axis) and on/off ratio (blue squares and dashed line, right axis) as a function of L_{Ch}. **d**, Width-normalized device g_m (black circles and solid line, left axis) and G_{ON} (blue squares and dashed line, right axis) as a function of L_{Ch}. Error bars represent s.d. of $n = 4$ devices.

Full-coverage semiconducting carbon nanotube arrays assembled based on the Langmuir–Schaefer method allow us to overcome this limitation. Here, we build nanotube thin-film transistors with scaled t_{ox} by transferring the semiconducting nanotube arrays onto a doped silicon substrate coated with a 5 nm HfO_2 gate dielectric, and defining source/drain electrodes by electron-beam lithography (EBL) and lift-off. Figure 3a presents the transfer characteristics of 10-μm-wide devices with three different values of L_{Ch}. The adoption of 99% purity semiconducting nanotubes dramatically improves the on/off ratio of the device source–drain current (I_{DS}) compared with that of control devices built with unsorted nanotubes or lower-purity semiconducting nanotubes, allowing a ratio greater than 1,000 to be achieved for devices with $L_{Ch} = 10$ μm, despite the extremely high tube density (Supplementary Fig. S7). Figure 3b shows a well-behaved output characteristic for a device with $L_{Ch} = 10$ μm (good linearity for source-to-drain bias (V_{DS}) $\ll$ gate-to-source bias (V_{GS}) and saturation for $V_{DS} \gg V_{GS}$). Figure 3c summarizes μ_{eff} calculated by considering the nanotube arrays as a full-coverage thin film, and also the measured on/off ratio as a function of L_{Ch}. The degradation of the on/off ratio for devices with shorter L_{Ch} is a result of the increase in the number of purely metallic pathways between source/drain electrodes with decreasing L_{Ch}, which can be quantitatively described with percolative modelling[18]. The high off-state leakage current for devices with short L_{Ch} can be further suppressed by the adoption of starting materials with even higher semiconducting nanotube purity. The values of μ_{eff} are in the range ~15–25 cm^2 V^{-1} s^{-1}, which is limited by inter- or intra-layer side-by-side nanotube junctions and is comparable to values from previous reports on thin-film transistors based on enriched semiconducting carbon nanotubes[5–7,19]. The combination of high C_i and μ_{eff} improves device performance significantly. As shown in Fig. 3d, for 1.5-μm-long devices an on-state conductance (G_{ON}) as high as 19 μS μm^{-1} and transconductance (g_m) as high as 5 μS μm^{-1} are achieved with $V_{DS} = -0.5$ V. Both g_m and G_{ON} are about eight times better than the values for previously reported semiconducting nanotube-enriched array devices with comparable device geometry but much lower tube density in the range ~10–20 tubes/μm (ref. 6). This improvement is also quantitatively consistent with previous analysis of C_i. An important figure of merit for thin-film transistors that directly determines I_{DS} and power consumption is the device on-state sheet resistance ($R_{S,ON}$). Our devices with $L_{Ch} = 10$ μm can achieve an average $R_{S,ON}$ of 44 ± 8 kΩ sq^{-1} with an on/off ratio above 1×10^3, almost four

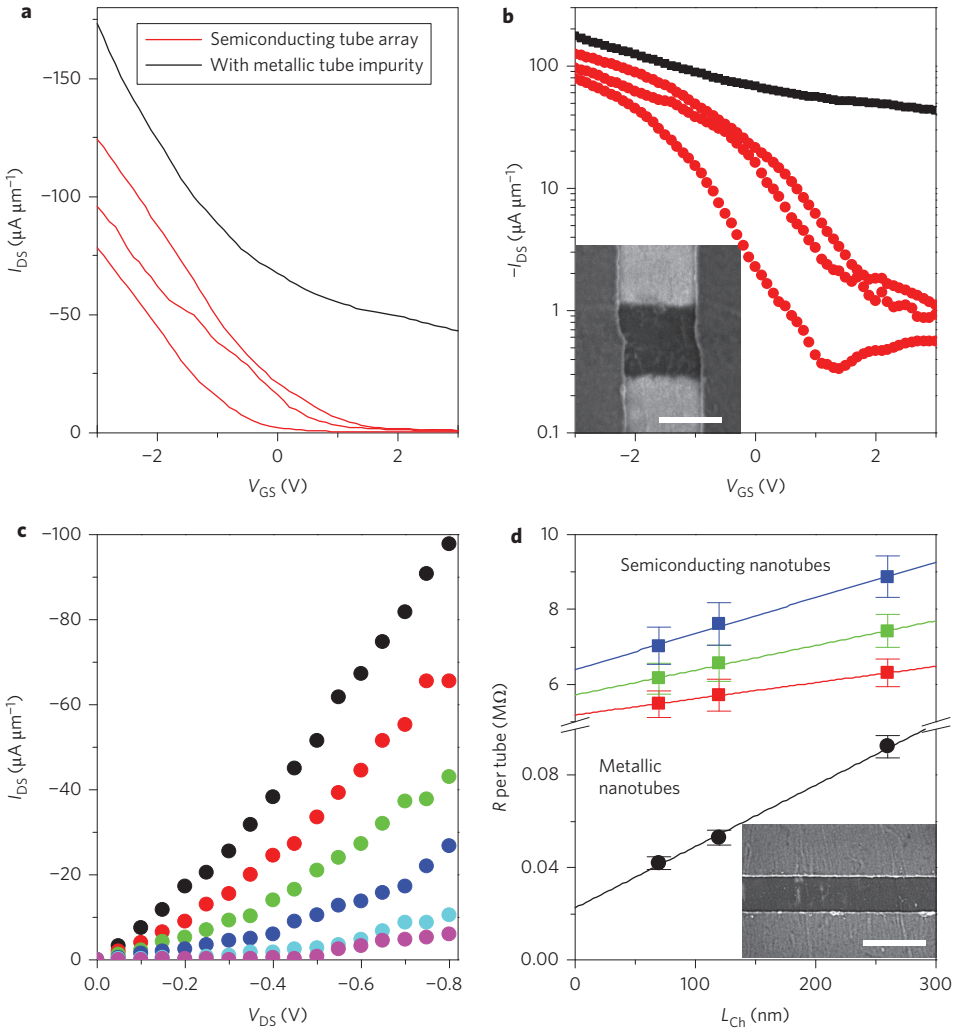

Figure 4 | Electrical properties of field-effect transistors that use 99% purity full-coverage semiconducting nanotube arrays and operate in direct transport regime. a,**b**, Transfer characteristics in linear (**a**) and logarithmic (**b**) scales for three nanotube field-effect transistors that incorporate purely semiconducting carbon nanotube arrays as a channel (red) out of 24 identical devices fabricated on the same substrate. Transfer characteristics of a typical device based on arrays with metallic nanotube impurities are also shown (black). Device channel widths are 100 nm and $L_{Ch} = 120$ nm. Applied $V_{DS} = -0.5$ V. Inset to **b**: SEM image of a device with width = 100 nm. Scale bar, 100 nm. **c**, Current–voltage characteristic of a nanotube field-effect transistor based on arrays of purely semiconducting nanotubes as shown in **a** and **b**. Applied V_{GS} changes from −2.5 V to 2.5 V with a step of 1 V from top to bottom. **d**, Averaged resistance R as a function of L_{Ch} for each semiconducting nanotube (squares) under $V_{GS} = -3$ V (blue), −2.5 V (green) and −2 V (red) (top to bottom), and for each metallic nanotube (black circles). Solid lines represent linear fits. Error bars represent s.d. of $n = 8$ devices. Inset to **d**: SEM image of a device with width = 10 μm. Scale bar, 200 nm.

times lower than the value reported in a previous publication[6] and representing one of the best reported so far for carbon nanotube thin-film transistors suitable for active matrix or logic applications[3,12–16]. Further improvement is still possible by adding a length-sorting step before the Langmuir–Schaefer assembly to increase the average nanotube length in the starting material; this can reduce the average number of tube–tube junctions per transport pathway and lead to an up to 10 times increase in μ_{eff} (ref. 15).

Although the current Langmuir–Schaefer method does not provide end-to-end registry of nanotubes, for devices with L_{Ch} much smaller than the average tube length, most nanotubes inside aligned arrays directly bridge source/drain electrodes, and devices can be viewed as conventional field-effect transistors, where electron transport is limited by scattering along the channel and the combined parasitic resistances at the contacts ($2R_C$), with effects from tube–tube junctions neglected. Such devices are expected to offer performances superior to silicon technologies based on a simple projection from the performance of individual nanotube devices[20]. However, realistic systems are more complicated, especially at extremely scaled nanotube pitch separation, where effects including screening[21] and Coulomb interactions[22] among neighbouring nanotubes must be considered. Direct experimental results are lacking, owing to the difficulties associated with obtaining extremely dense aligned arrays of virtually all semiconducting carbon nanotubes. The high-purity semiconducting nanotube arrays generated by the Langmuir–Schaefer method allow us to study the electrical properties of nanotubes with both scaled pitch separation and device dimension. Figure 4a,b plots the transfer curves of devices built on a 10 nm HfO_2 gate dielectric with $L_{Ch} = 120$ nm and width = 100 nm, where each device incorporates only about 110 nanotubes so that certain devices may contain only semiconducting nanotubes (Fig. 4b, inset). The presence of even one metallic nanotube in a channel is easy to tell as it will severally degrade the device on/off ratio and lead to an off-state current that is unacceptable for logic electronics. With the present 99% purity semiconducting nanotube solution as the starting material, we can achieve a ~10–20% yield

(3 out of 24 for this particular chip, suggesting a semiconducting nanotube purity above 98%) of fabricated devices that are composed of purely semiconducting nanotubes, as evident from their demonstrated high on/off ratios. These devices show that the extremely scaled nanotube pitch does not affect their operation. The large subthreshold swing could be caused by the wide distribution of threshold voltage of individual nanotubes resulting from variations in nanotube diameter and/or the presence of surface charges (Supplementary Fig. S8). The devices built on arrays with only semiconducting nanotubes exhibit the highest g_m (>40 μS μm^{-1}) and current density (125 μA μm^{-1}) yet reported, representing a threefold increase over devices built with identical geometry, but with CVD-grown nanotube arrays with a moderate tube density of ~4 tubes/μm (with the same V_{DS}) (ref. 23). Although the improvement is impressive, it is lower than expected, even after taking into account the screening effect[17,21], giving several times lower μ_{eff} in our devices. The current–voltage characteristics plotted in Fig. 4c suggest that the μ_{eff} could be limited by a substantial Schottky barrier at the carbon nanotube–metal contacts. A standard transmission-line method was used to extract $2R_C$, the intrinsic field-effect mobility of semiconducting nanotubes (μ_{FE}) and the resistivity (resistance per unit length) of metallic nanotubes (ρ_m), as shown in Fig. 4d. The contribution to I_{DS} from metallic and semiconducting nanotubes can be analysed separately by assuming that ρ_m is independent of V_{GS} and that the resistances of the transport pathways associated with each of the tubes add in parallel[24]. Devices with a much wider width (10 μm), as shown in the inset to Fig. 4d, were used to minimize device variations. With a semiconducting nanotube purity of ~99% and full surface coverage, the extracted $2R_C$ and ρ_m of the metallic nanotubes were 22 ± 2 kΩ/tube and 270 ± 20 kΩ μm^{-1}, respectively. These values are comparable to those extracted from individual nanotube devices with similar sub-micrometre L_{Ch} and made from the same nanotube source; that is, $2R_C$ = 9 ± 2 kΩ/tube and ρ_m = 200 ± 10 kΩ μm^{-1} (ref. 25). For semiconducting nanotubes, the extracted μ_{FE} is 130 ± 20 cm^{2}V^{-1} s^{-1}, only somewhat lower than that of individual solution-processed nanotubes (~300 cm^{2}V^{-1} s^{-1}) (ref. 25), indicating that their channel transport property is not affected by this extremely scaled nanotube pitch separation. It is worth noting that although the μ_{FE} of solution-processed semiconducting nanotubes is almost 10 times lower than that of CVD tubes[24], possibly due to additional scattering from structural defects induced during nanotube suspension and purification processes, for ultimately scaled nanotube transistors operating in the quasi-ballistic regime, device performance is only limited by nanotube quantum resistance plus parasitic contact resistance, instead of channel resistance or μ_{FE}. Therefore, solution-processed nanotubes will offer a performance similar to that of CVD tubes in those ultra-scaled transistors despite their lower μ_{FE}, together with excellent short channel control compared to silicon devices resulting from the intrinsic ultra-thin body of single-walled carbon nanotubes. On the other hand, the $2R_C$ of semiconducting nanotubes inside the array is over 100 times higher than that of individual nanotubes (5.8 ± 0.6 MΩ/tube versus 40 ± 20 kΩ/tube), and can be modulated significantly by V_{GS}, indicating the existence of a large Schottky barrier at the contacts. This high contact resistance may be explained by the small exposed contact area for each nanotube resulting from the extremely dense packing and poor wetting of metals on a full-coverage carbon surface[20,26], the lowering of the valance band of nanotubes at the contacts due to inter-tube Coulomb interactions[22], together with minor contributions from factors including currently unoptimized device structure (Supplementary Fig. S9) and residual amorphous carbon remaining from the surfactant. The degradation of the contacts due to nanotube pitch scaling suggested in theoretical work[22] and observed in our experiments could be one of the principal challenges to the realization of high-performance nanoelectronics based on carbon nanotubes. Research on finding solutions to this limitation, such as additional surface treatment of the nanotubes located within the contact area (Supplementary Fig. S10), is under way. Even with large $2R_C$, a cutoff frequency above 10 GHz has been achieved by integrating the semiconducting nanotube arrays into a radiofrequency device with embedded gate and a 300 nm-long channel, which is among the best values reported so far for nanotube radiofrequency transistors with complete contact and finger metallization (Supplementary Figs S11 and S12)[27,28].

In summary, densely packed, aligned arrays of 99% pure semiconducting single-walled carbon nanotubes with near full surface coverage were assembled using a Langmuir–Schaefer method, and their structures were characterized in detail by SEM, AFM, TEM and polarized Raman spectroscopy. The high nanotube density, semiconducting nanotube purity and quality of alignment lead to improved electrical properties for devices integrating carbon nanotube channels. The extreme pitch scaling of the nanotube separation does not affect the intrinsic properties of the nanotubes, thereby showing promise for using single-walled carbon nanotube arrays in both high-performance thin-film electronics and post-silicon technologies. Improvement in the electrical contact between the nanotube arrays and metal electrodes, further optimization of the nanotube electronic type and diameter separation techniques, reduction of interface traps for better device consistency, together with complementary metal–oxide–semiconductor-compatible circuit- and system-level implementation, represent some of the most important subjects for future work, where the main challenges lie in the requirement for extreme engineering control rather than the intrinsic limitations of the material or processes. Meanwhile, the scalability of the Langmuir–Schaefer assembly process, together with the high-performance capability of assembled semiconducting nanotube arrays, make this technique valuable for a range of other emerging applications that use large collections of nanotubes, such as transparent electronics and stretchable electronics.

Methods

Preparation of 99% purity semiconducting carbon nanotube aqueous solution. Single-walled carbon nanotubes synthesized by the arc-discharge method and purified by both heat and acid treatments (Hanwha Nanotech, ASP-100F) were dispersed in an aqueous solution of 1 wt% sodium dodecyl sulphate (SDS) by sonication with a high-power horn sonicator (30 min, 600 W, 20% amplitude, 20 kHz) followed by centrifugation (17,000*g* for 1 h, Beckman Coulter, Optima L-100 XP ultracentrifuge) to remove sediments. The nanotube solution was further purified in a step-gradient centrifuge stage using 30% iodixinol (Sigma-Aldrich) solution with 0.25% SDS as a stopping layer at 287,700*g* for 18 h, to remove large agglomerates of nanotubes. It is important to note that the centrifugation step is only used to remove graphitic impurities and not to sort nanotubes by electronic type. Electronic type sorting was performed by passing the nanotube solution through a chromatographic column loaded with Sephacryl-200 (ref. 29). The solution passed through the column and separated into two distinct bands. The first band, blue-green in colour, consisted of metallic nanotubes and the latter, red in colour, was predominately semiconducting. The semiconducting nanotube purity of 99% was confirmed by both absorption spectroscopy and direct electrical characterization. Further enhancement of semiconducting nanotube purity to above 99.99% is possible with more refined engineering control of the separation processes, especially with the development of orthogonal and/or iterative separation schemes[30]. At present, the biggest challenge is not necessarily the separation techniques themselves, but the lack of reliable and high-throughput analytical techniques to detect the exact amount of residual metallic nanotube impurities and provide timely feedback to further improve the separation processes.

Preparation of 99% purity semiconducting nanotube DCE solution. The 99% pure semiconducting nanotube aqueous solution was filtered through a mixed cellulose ester membrane (MF-Millipore Membrane, mixed cellulose esters, hydrophilic, 0.1 μm, 25 mm) and washed with copious amount of deionized water to remove residual SDS surfactant. Nanotubes were then resuspended in 2 wt% poly(*p*-phenylenevinylene-co-2,5-dioctyloxy-*m*-phenylenevinylene (PmPV, Sigma-Aldrich) in DCE (>99.0%, Sigma-Aldrich) solution by sonication with a high-power horn sonicator (60 min, 600 W, 95% amplitude, 20 kHz) followed by centrifugation (210,000*g* for 2 h, Beckman Coulter, Optima L-100 XP ultracentrifuge) to remove precipitants. The supernatant was collected, filtered through Teflon filter paper

(Fluopore, 0.22 μm pore), and resuspended in clean DCE. These filtration and resuspension processes were performed for several cycles to remove the excess PmPV molecules[9]. The final suspension was sonicated again with the high-power horn sonicator for 10 min before use.

Langmuir–Schaefer assembly of aligned nanotube arrays. A volume of 180 μl of 99% purity semiconducting nanotube DCE solution was dispersed dropwise on the water surface of a Langmuir trough (Model 611, Nima Technologies) placed on top of an optical table, and compressed to a target pressure around 30 mN m^{-1} with a bar moving rate of 20 cm^2 min^{-1} under multiple (~15) isothermal cycles. Each isothermal cycle lasted on average ~8 min, including compression and expansion processes. Compression was halted when the nanotube film began to crack with a further increase of surface pressure. The stopped position is very reproducible for volumes taken from a single batch of nanotube solution, which therefore have identical semiconducting nanotube concentrations. The assembled semiconducting nanotube arrays were then horizontally transferred onto the receiving substrates using the Langmuir–Schaefer method.

Device fabrication. After transferring the semiconducting nanotube arrays to a substrate comprising either heavily doped silicon to act as a global back gate or an embedded tungsten electrode to act as a local bottom gate, the whole substrate was annealed under vacuum with a base pressure of less than 1×10^{-6} torr at 400 °C for 2 min to remove the PmPV wrapped around the nanotubes. The first EBL step was performed to expose the contact pad area for source/drain electrodes in the poly(methyl methacrylate) (PMMA) resist. A subsequent oxygen plasma etching removed the nanotubes that would otherwise be under the contact pads, preventing mechanical damage to the contact pads during probing caused by poor adhesion of the nanotube film on the oxide surface. Another EBL step was then performed to define the source/drain electrodes by opening windows in the PMMA resist. ultraviolet–ozone treatment was performed for 2 min to slightly oxidize the carbon nanotubes under the contact area, which reduces parasitic $2R_C$ by improving the wetting of metals on the nanotube surface. Source/drain electrodes were then formed by lift-off of the electron beam-evaporated titanium (0.2 nm)/palladium (15 nm)/gold (20 nm). A final EBL step was performed to pattern hydrogen silsesquioxane (HSQ)/PMMA bilayer resist into etch masks covering the active area of each device. A subsequent oxygen plasma etching defined the device width and electrically isolated the devices from one another. After stripping the photoresist with hot acetone, devices were measured at room temperature in air without further treatments. The structural quality and density of the assembled nanotube arrays were not affected by these device fabrication processes, as confirmed by Raman spectroscopy (Supplementary Fig. S13).

Instrumentation. SEM images were taken with a Zeiss/LEO 1560 microscope. AFM images were acquired with a Dimension 3000 instrument in tapping mode. TEM images were obtained using a JEOL 3000F transmission electron microscope. Cross-sectioned samples were prepared using a FEI Helios 400S dual-beam focused ion beam instrument. Polarized Raman spectra were measured using a LabRAM ARAMIS micro-Raman instrument with an excitation wavelength of 532 nm and a spot size of ~1 μm^2, by rotating the substrate with fixed polarization of the incident laser beam. Optical absorption measurements of the carbon nanotube arrays transferred onto glass substrates were performed with a Perkin Elmer Lambda 950 ultraviolet–visible spectrometer. A Leica Vb6 electron beam writer was used to pattern the photoresist. Direct current and radiofrequency characterizations were carried out in a probe station using an Agilent B1500 parameter analyser and a E8364C network analyser in air at room temperature.

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Author contributions

Q.C. conceived and designed the experiments. Q.C. and S.J.H. performed the experiments and analysed the data. G.S.T. purified the nanotubes. Y.Z. performed TEM imaging. D.D. Lu performed the Technology Computer-Aided Design simulation. Q.C. wrote the manuscript. All authors discussed the results and commented on the manuscript.

Additional information

Supplementary information is available in the online version of the paper. Reprints and permission information is available online at http://www.nature.com/reprints. Correspondence and requests for materials should be addressed to Q.C.

Competing financial interests

The authors declare no competing financial interests.