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Flexible CMOS integrated circuits based on carbon nanotubes with sub-10 ns stage delays

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High-performance logic circuits that are constructed on flexible or unconventional substrates are required for emerging applications such as real-time analytics. Carbon nanotube thin-film transistors (TFTs) are attractive for these applications because of their high mobility and low cost. However, flexible nanotube TFTs usually suffer from much lower performance than those built on rigid substrates, and the resulting flexible integrated circuits typically exhibit low-speed operation with logic gate delays of over 1 µs, which severely limits their practical application. Here we show that high-performance carbon nanotube TFTs and complementary circuits can be fabricated on flexible polyimide substrates using a high-yield, scalable process. Our flexible TFTs exhibit state-of-the-art performance with very high current densities (>17 µA µm^{-1}), large current on/off ratios (>10^6), small subthreshold slopes (<200 mV dec^{-1}), high field-effect mobilities (~50 cm^2 V^{-1} s^{-1}) and excellent flexibility. We also develop a reliable n-type doping process, which allows us to fabricate complementary logic gates and integrated circuits on flexible substrates. With our approach, we build flexible ring oscillators that have a stage delay of only 5.7 ns.

Carbon nanotubes (CNTs) are a promising replacement for silicon in scaled complementary metal–oxide–semiconductor (CMOS) technology[1,2]. Research in the field has led to considerable progress in areas such as transistor scaling[1,2], contact engineering[3,4] and improved semiconducting tube purity and placement[5–9]. However, if CNT-based logic technology is to be pushed further, more work is required in order to demonstrate that the technology can offer sufficient performance benefits on a circuit and systems level compared with its silicon counterpart[9,10]. Thin-film transistors (TFTs), on the other hand, have less stringent requirements in terms of performance and scaling than logic technology, and flexible nanomaterials such as CNTs could offer appealing advantages over rigid silicon[11]. TFTs have a broad range of applications in areas such as displays and flexible devices, and several channel materials have been extensively studied, including amorphous silicon[12], organic/oxide semiconductors[13,14], CNTs[15] and two-dimensional layered materials[16]. CNTs, in particular, have been recognized as an attractive candidate for making low-cost high-performance TFTs due to their high mobility, excellent durability and easy processing[11,17].

When evaluating TFT performance, carrier mobility μ, current on/off ratio I_{on}/I_{off}, and on current density J_{on} are usually considered the three most important metrics. In the presence of metallic tubes (even at small percentages), Jon and I_{on}/I_{off} have an undesired tradeoff with channel length, which makes it challenging to improve TFT performance by simple scaling[18]. In general, flexible CNT TFTs typically exhibit much lower performance (for example, J_{on} typically below 1 µA µm^{-1}; refs [18–28]) than those on rigid substrates (Jon in the range ~1–100 µA µm^{-1}; refs [29,30]). This is mainly due to the process limitations for flexible substrates, such as substrate cleanliness, process temperature and lithography resolution. As a result, flexible CNT circuits are relatively slow. For example, CNT-based flexible ring oscillators (ROs) usually have stage delays longer than 1 µs (or output oscillation frequencies below 100 kHz), and such low performance and operation speed severely limit their practical applications[31]. In addition, most flexible CNT TFTs reported so far are unipolar p-type field-effect transistors (PFETs), whereas CMOS logic is highly desired for low-power applications.

In this Article, we demonstrate a reliable process to fabricate high-speed CNT CMOS integrated circuits on flexible substrates with high yield. Using highly purified CNTs (semiconducting purity > 99.99%), the flexible CNT TFTs achieve a high J_{on} of ~17.2 µA µm^{-1}, while maintaining a large I_{on}/I_{off} of >10^6; the performance of these devices is on a par with the best reported values for rigid CNT TFTs[29–31]. We also fabricate flexible CNT CMOS ROs, which exhibit a record-high oscillation frequency of 17.6 MHz, equivalent to a stage delay of only 5.7 ns.

High-performance flexible CNT TFTs

As illustrated in Fig. 1a, back-gated CNT TFTs were fabricated by standard photolithography on flexible polyimide substrates, where the local back gate consisted of a Ti/Pd/Ti stack. This was followed by atomic layer deposition (ALD) of 40 nm Al_2O_3/10 nm HfO_2 at 150 °C as the gate oxide[18]. The equivalent relative dielectric constant was estimated to be $\varepsilon_r = 6.27$ from capacitance measurements on a control sample with the same oxide stack. A self-assembled monolayer (SAM) of chloro(dimethyl)octadecylsilane was used to functionalize the oxide surface for high-density CNT deposition. Ti/Pd was used as source–drain metal contacts, and TFT channels were patterned with a width of $W_{ch} = 10$ µm and different lengths of $L_{ch} = 2,3,5$ and 8 µm. After fabrication, the polyimide film was peeled off from the handling wafer, yielding flexible CNT TFTs (Fig. 1b). Figure 1c presents a scanning electron microscopy (SEM) image of the deposited high-density CNT network, where the tube density (~100 tubes per µm^2) was significantly improved over our previous work[18]. The average CNT length is ~1 µm (Supplementary Fig. 1). Here, semiconducting CNTs were isolated using a polymer extraction technique as reported previously[9]. Figure 1d shows the UV–vis–NIR absorption spectrum of the polymer-sorted CNT solution, where the strong S_{22} absorbance peak (the second optical transition from semiconducting tubes) and the completely attenuated M_{11} peak (the first optical transition from metallic tubes) indicate

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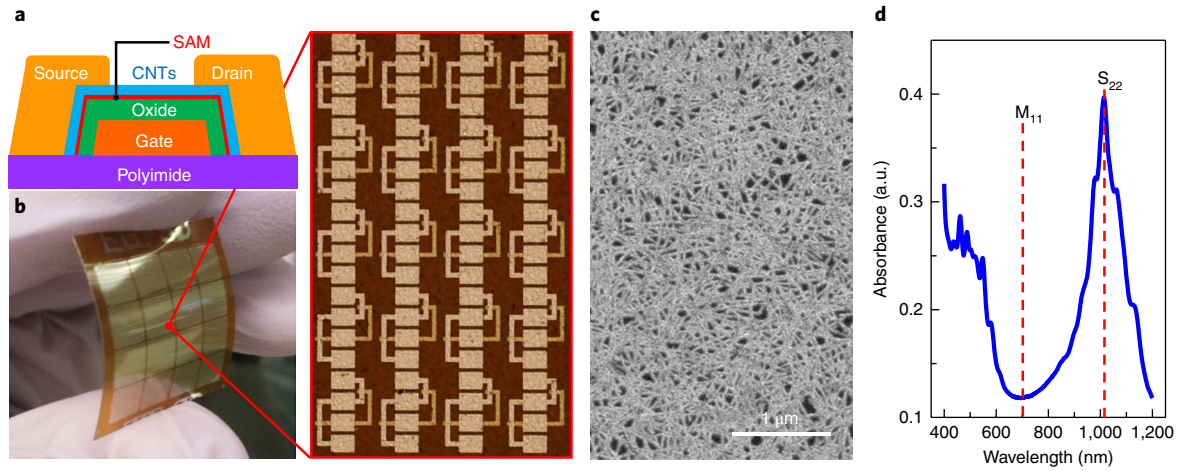

Fig. 1 | Fabrication of flexible CNT TFTs. a, Schematic illustration of the device structure of a back-gated TFT. The gate metal comprises a stack of 2 nm Ti/50 nm Pd/1 nm Ti. The gate dielectric consists of 40 nm Al_2O_3 and 10 nm HfO_2, whose surface is functionalized with a self-assembled monolayer (SAM) of chloro(dimethyl)octadecylsilane for CNT deposition. The source–drain contact is composed 0.2 nm Ti/70 nm Pd. **b**, Photograph of CNT TFTs fabricated on a flexible polyimide substrate. Inset: microscope image of TFT arrays. **c**, SEM image of the deposited high-density CNT random network. **d**, UV–vis–NIR absorption spectrum of the polymer-sorted CNT solution. The strong S_{22} absorbance peak and the completely attenuated M_{11} peak indicate high semiconducting purity.

a high semiconducting purity greater than 99%. In addition, a separate electrical testing on more than 20,000 CNT transistors was used to further quantify the solution purity to be over 99.99% (Supplementary Fig. 2). The high CNT density and ultrahigh semiconducting purity are one of the key ingredients to achieve high-performance flexible CNT TFTs in this work.

The fabricated TFTs were measured on a semi-automated probe station at room temperature, which allowed us to investigate the device statistics from hundreds of TFTs. Figure 2a presents the I_{ds}–V_{gs} transfer curves at $V_{ds} = -0.5$ V for 250 CNT TFTs with $L_{ch} = 2$ μm and $W_{ch} = 10$ μm. As-fabricated TFTs are naturally PFETs because of unintentional p-doping from oxygen or moisture in air. This sample showed nearly 100% device yield (250 of 256 devices) and relatively small device-to-device variation (Supplementary Fig. 3), suggesting the feasibility of our process for large-scale TFT fabrication. The I_{ds}–V_{ds} output curves plotted in Fig. 2b show that we achieved an exceptionally high current density of $J_{on} = I_{ds}/W_{ch} = 17.2\ \mu A\ \mu m^{-1}$, even under relatively small bias ranges ($V_{ds} = -3$ V, $V_{gs} = -3$ V) for flexible TFTs. This number is orders of magnitude higher than reported in the literature for flexible CNT TFTs (typically ~0.01–1 $\mu A\ \mu m^{-1}$)[18–28], and is more comparable with the best values obtained for those on rigid substrates (typically ~1–100 $\mu A\ \mu m^{-1}$)[29,30]. It is noted that such a comparison is intended for TFTs with a similar channel length range (~2–100 μm), and there are reports of even higher current densities (>100 $\mu A\ \mu m^{-1}$) on rigid substrates with sub-micrometre channel length[32,33]. Also, the linear I_{ds}–V_{ds} relation at small V_{ds} suggests the absence of a Schottky barrier at the source–drain contacts. Figure 2c plots the corresponding I_{ds}–V_{gs} transfer curve at $V_{ds} = -0.5$ V of a representative TFT, showing a high I_{on}/I_{off} of ~2×10^6 and a quite small subthreshold slope of SS = 180 mV dec^{-1} (typical literature values are >200 mV dec^{-1}), even with a relatively thick gate oxide stack. As discussed earlier, the presence of metallic tubes usually makes it difficult to improve both J_{on} and I_{on}/I_{off} by shrinking the TFT channel length[18]. For comparison, Fig. 2d plots J_{on} versus I_{on}/I_{off} for flexible CNT TFTs reported in the literature as well as the results from this study; this highlights the fact that our approach offers a high current density while maintaining a large I_{on}/I_{off} ratio, which is mainly attributed to the high semiconducting CNT purity. To calculate the carrier mobility, the gate capacitance C_{ox}, which in practice is difficult to measure accurately for CNT TFTs, can be first estimated using the parallel plate model: $C_{ox} = \varepsilon_0\varepsilon_r/t_{ox}$ (upper limit), considering the high density of the CNT network and relatively thick gate oxide (oxide thickness larger than tube spacing)[34]. With the extracted transconductance of $g_m = 14.6\ \mu S$ from Fig. 2c, it is estimated that $\mu = \frac{g_m L_{ch}}{V_{ds} C_{ox} W_{ch}} = 52.6\ cm^2\ V^{-1}\ s^{-1}$ (lower limit). Statistical analysis of 250 devices in Fig. 2a yields $\mu = 55 \pm 9\ cm^2\ V^{-1}\ s^{-1}$, which falls into the upper range of typical reported mobility values for CNT TFTs (~1–100 $cm^2\ V^{-1}\ s^{-1}$)[18–30].

To further understand the carrier transport in CNT TFTs and its dependence on the device dimensions, Fig. 2e plots the on current and field-effect mobility as a function of L_{ch}. For a fair comparison, we extract the device on current at a constant gate overdrive (for example, $|V_{gs} - V_t| = 1$ V where V_t is the threshold voltage), denoted $I_{on,1VOD}$. It is found that $I_{on,1VOD}$ decreases with increasing L_{ch}, which is consistent with percolation transport in TFTs[18]. The extracted mobility shows a relatively weak dependence on L_{ch}, but is expected to increase dramatically as L_{ch} is further scaled down close to the tube length (~500 nm), approaching the direct-contact transport regime[2,32,33]. Furthermore, to test the durability of our CNT TFTs on flexible polyimide substrates, the sample was mounted onto glass tubes with different radii, $R = 50$, 20, 8 and 5 mm, for bending tests. Figure 2f plots the I_{ds}–V_{gs} transfer curves at $V_{ds} = -0.5$ V of a representative CNT TFT under different bending radii, showing no degradation on the device performance (Supplementary Fig. 4). Here the smallest bending radius of $R = 5$ mm corresponds to a bending-induced tensile strain of about $\varepsilon = 0.5 t_{sub}/R = 1.27\%$ (polyimide substrate thickness $t_{sub} = 127$ μm). These results demonstrate the excellent flexibility of our CNT TFTs, which is also very important for building high-performance flexible electronics.

Reliable n-type doping for flexible CMOS logic

For low-power applications, complementary logic is highly preferred, although as-fabricated CNT TFTs are naturally PFETs. In a short-channel CNT transistor ($L_{ch} < L_{CNT}$, that is, direct-contact transport), the workfunction of source–drain contacts filters the carrier type being injected into the channel and hence determines the transistor polarity. As a result, low-workfunction metals (for example, Sc and Er) are used as direct contacts to make CNT NFETs. In contrast, the carrier transport in CNT TFTs ($L_{ch} \gg L_{CNT}$,

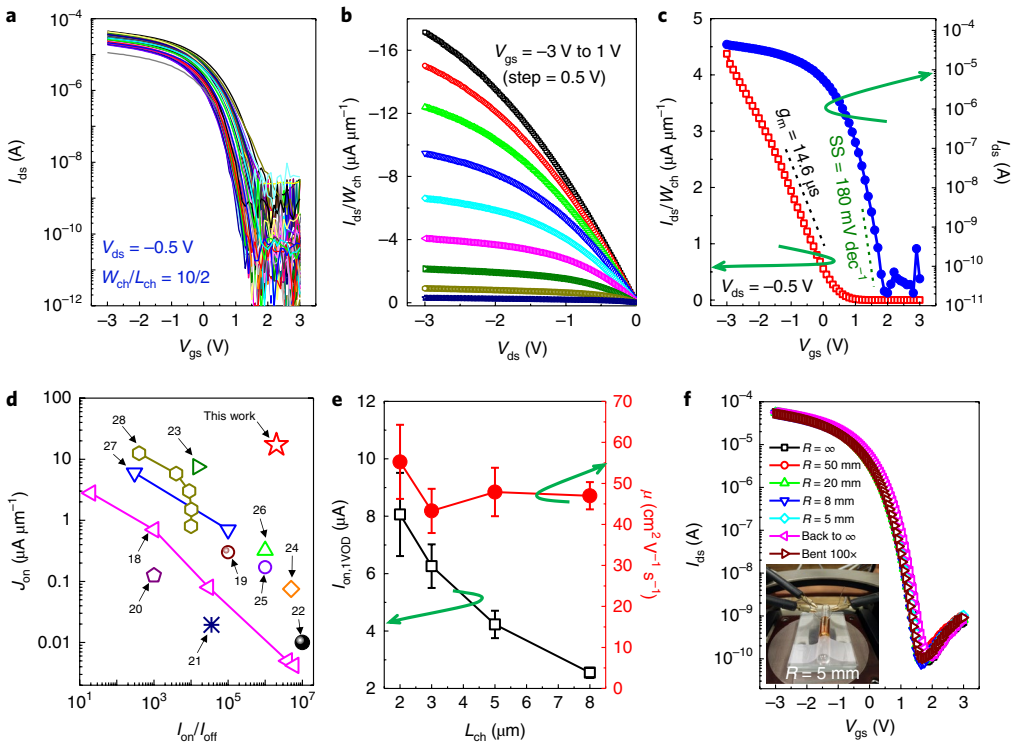

Fig. 2 | Flexible CNT TFTs. a, I_{ds}–V_{gs} transfer curves at V_{ds} = −0.5 V for 250 CNT TFTs with channel length L_{ch} = 2 μm. **b**, Set of I_{ds}–V_{ds} output curves from an individual TFT, showing a large on current density of >17 μA μm^{-1}. **c**, Corresponding I_{ds}–V_{gs} curve at V_{ds} = −0.5 V, showing a high I_{on}/I_{off} ratio above 10^6, small subthreshold slope of SS = 180 mV dec^{-1} and high transconductance of g_m = 14.6 μS, yielding a field-effect mobility of μ = 52.6 cm^2 V^{-1} s^{-1}. **d**, Plot of current density J_{on} versus I_{on}/I_{off} ratio to compare representative flexible CNT TFTs reported in the literature. Our work shows the highest current density while maintaining a large I_{on}/I_{off} ratio. **e**, Extracted on current under a constant gate overdrive of $|V_{gs} - V_t|$ = 1 V ($I_{on\text{-}1VOD}$, left axis) and carrier mobility (right axis) for CNT TFTs with different channel lengths from 2 to 8 μm. Error bars represent standard deviations from 250 TFTs for each channel length. **f**, I_{ds}–V_{gs} transfer curves at V_{ds} = −0.5 V for a typical CNT flexible TFT bent under different radii R, showing no degradation on device performance with R down to 5 mm. $R = \infty$ indicates no bending (the sample is laid flat) during measurement. Inset: photograph of the sample mounted on a glass tube with a diameter of 10 mm.

that is, percolation transport) is usually dominated by tube-to-tube junctions rather than contacts. Therefore, n-type channel doping is usually adopted to make CNT NFETs (although some recent work has demonstrated n-type TFTs by using Sc as source–drain contacts[35]), as illustrated in Fig. 3a. In the literature, many organic molecules and dielectric films (for example, Si_3N_4, Al_2O_3 and HfO_2) have been investigated as n-type doping sources for CNT TFTs[22,36–40]. Among them, organic molecules may suffer from poor stability and process compatibility issues, and plasma damage of CNTs was found during the plasma-enhanced chemical vapour deposition of Si_3N_4 (ref. [41]). By comparison, ALD oxide passivation on CNTs provides a simple and harmless approach for effective n-type doping (from oxygen vacancies)[38–40], and it is also readily process-compatible for building CMOS logic.

Here, we have performed a systematic study on the doping effect of various ALD layers, with the results summarized in Fig. 3b. It is found that ALD-Al_2O_3 passivation alone does not provide sufficient n-type doping to fully convert initial PFET to unipolar NFET, and the resulting TFT is ambipolar. To further aid the conversion, a nominally 2-nm-thick Al layer was first evaporated on the sample surface prior to ALD, which was readily oxidized in air into AlO_x (ref. [39]). The formed native AlO_x served as a seeding layer for the subsequent ALD process to ensure better coverage on CNTs, and also contributed to the n-type doping. By combining 2 nm Al evaporation and 40 nm Al_2O_3 ALD, unipolar NFET was successfully achieved with a similar performance as the initial PFET, where the high I_{on}/I_{off} ratio of >10^6 was preserved. The n-type doping layer also served as an effective passivation layer to significantly reduce the hysteresis in NFET and showed excellent stability over time (more NFET data are shown in Supplementary Figs. 5–8). In this approach, reducing the ALD-Al_2O_3 thickness (from 40 nm to 30 or 20 nm) was found to weaken the n-type doping effect, leading to ambipolar TFTs. Figure 3c plots the I_{ds}–V_{ds} curves for an individual NFET. The linear I_{ds}–V_{ds} relation at small V_{ds} suggests that the sharp Schottky barrier at source–drain contacts is not limiting the carrier tunnelling transport.

By integrating the above bilayer n-type doping process for NFETs, we successfully demonstrate high-performance CNT CMOS logic gates on flexible substrates, including inverters, NAND and NOR gates. Figure 3d plots the output characteristics of a flexible CNT CMOS inverter, showing abrupt switching from V_{DD} = +3 V to V_{SS} = −3 V. As shown in the top inset, the high inverter gain is calculated to be about 25. We also achieved nearly 100% inverter yield (125 of 128 devices, Supplementary Fig. 9), indicating good reliability of our CMOS fabrication process on flexible substrates. The dashed boxes in the 'eye' pattern show a large inverter noise margin of ~2.2 V (more than 36% of $|V_{DD} - V_{SS}|$), which implies a large operation margin for cascade integrated circuits such as ring oscillators (ROs). Figure 3c,f plots the output characteristics of flexible CNT NAND and NOR gates, respectively, showing the correct Boolean functionalities. Here, the input signals are the voltage inputs for A and B, where logic '1' and '0' represent voltages V_{DD} = +3 V and V_{SS} = −3 V, respectively.

High-speed flexible CNT CMOS ROs

As shown in Fig. 4a, five-stage CNT ROs were also fabricated, where an additional stage of CMOS inverter was used as an output buffer

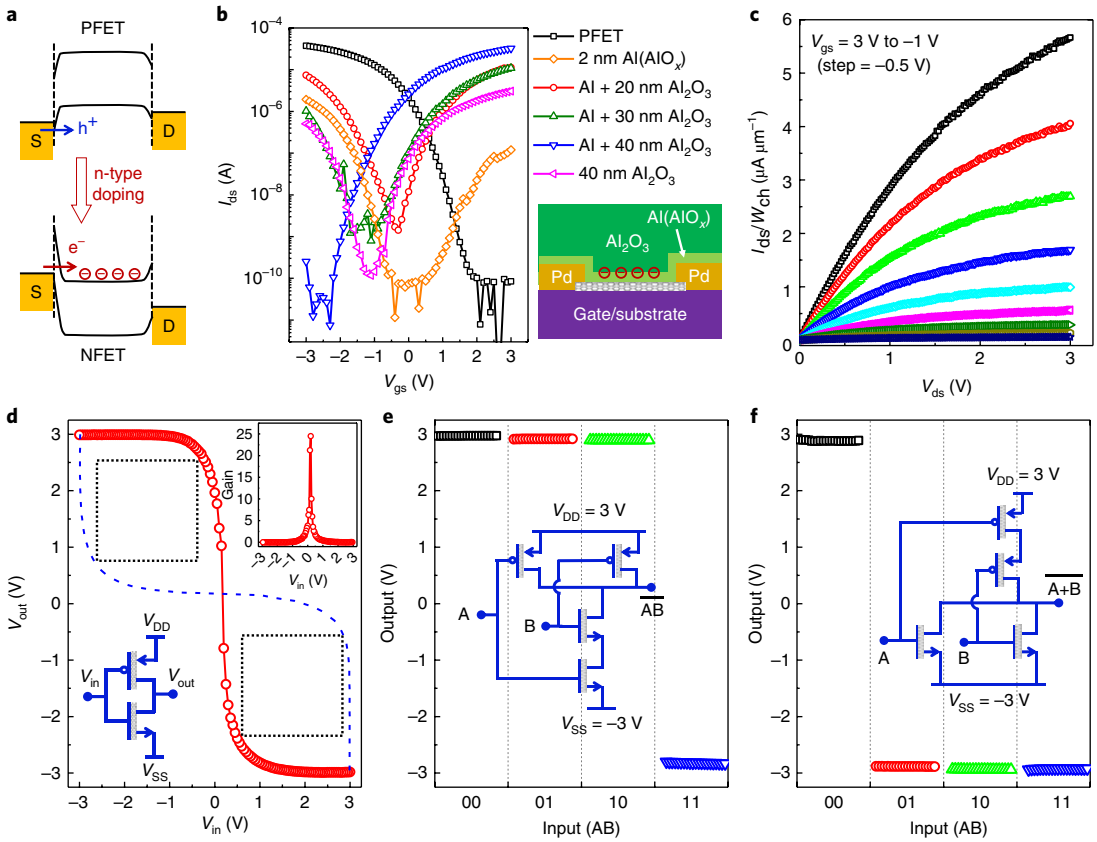

Fig. 3 | Flexible CNT complementary logic gates. a, Schematic illustration of n-type doping to convert a PFET into an NFET. **b**, I_{ds}–V_{gs} transfer curves at V_{ds} = 0.5 V of CNT TFT after depositing various doping layers. Inset: device structure. The starting 2-nm-thick Al layer, which is oxidized in air to AlO_x, acts as a seeding layer for the subsequent ALD of Al_2O_3 and also provides n-type doping to the CNT TFT channel. **c**, A set of I_{ds}–V_{ds} output curves of an n-type CNT TFT after doping. **d**, Output characteristic of a flexible CNT CMOS inverter, showing abrupt switching from V_{DD} = +3 V to V_{SS} = −3 V. Bottom inset: schematic diagram of CMOS inverter. Top inset: inverter gain of about 25. **e**, Output characteristic of a flexible CNT NAND gate. The input signals are the voltage inputs for A and B, where logics '1' and '0' represent voltages V_{DD} = +3 V and V_{SS} = −3 V, respectively. Inset: schematic diagram of CMOS NAND gate. **f**, Output characteristic of a flexible CNT NOR gate. Inset: schematic diagram of CMOS NOR gate.

for electrical measurements. Figure 4b presents the corresponding schematic circuit diagram. Figure 4c shows the output frequency spectrum at a supply voltage of V_{DD} = 6 V, featuring an oscillation frequency of f_O = 1.10 MHz. The stage delay in the flexible RO can be estimated as $\tau_{SD} = 1/(2Nf_O)$ = 90.9 ns, where N = 5 is the number of inverter stages. Such a sub-100 ns stage delay is faster than previous reports of CNT ROs on flexible substrates[25–27,42]. To investigate the effect of TFT dimension (for example, channel length L_{ch} and source–drain-to-gate overlap L_{ov}) on the oscillation frequency, we fabricated three types of RO: the fastest (5F) with L_{ch} = 3 μm and L_{ov} = 3 μm, the slowest (5S) with L_{ch} = 5 μm and L_{ov} = 5 μm, and the medium one (5M) with L_{ch} = 3 μm and L_{ov} = 5 μm. The results are summarized in Fig. 4d. It was found that reducing L_{ch} and L_{ov} increases the TFT drive current and reduces the parasitic capacitance, and hence improves f_O. Figure 4e shows that both oscillation frequency and amplitude are enhanced as V_{DD} is increased from 3 V to 6 V, which is another signature of digital RO. Figure 4f plots the voltage dependence of the oscillation frequency measured from two representative CNT ROs. To further improve f_O and reduce the stage delay to sub-10 ns, we made another sample with reduced channel length L_{ch} down to ~2 μm, pushing f_O to 5.42 MHz at V_{DD} = 10 V, as shown in Fig. 4g. Also, the HfO_2 gate oxide thickness was further increased to 20 nm, so that the device could sustain higher V_{DD}. As shown in the inset of Fig. 4g, the highest f_O we achieved in this study is 17.6 MHz at V_{DD} = 17 V, corresponding to a stage delay of only 5.7 ns. Figure 4h compares the stage delay among representative flexible ROs made with different nanomaterials, including CNTs, organic semiconductors, oxide semiconductors, nanocrystals and hybrid nanomaterials[22,25–27,43–48]. This highlights that fact that our flexible ROs, which offer stage delays down to sub-10 ns, are faster than previous reports on flexible systems, and are comparable to the best demonstrations on rigid substrates[31].

Conclusions

We have reported a scalable and reliable process to fabricate high-performance CNT TFTs and complementary circuits on flexible substrates with high yield. The flexible CNT TFTs exhibited state-of-the-art performance and excellent durability, with a bending radius down to 5 mm. To integrate complementary circuits on flexible substrates, we have also developed a reliable n-type doping process using evaporation of a thin Al layer followed by ALD of Al_2O_3. These process innovations, together with our highly purified CNT solution and high-density CNT deposition, led to the fabrication of flexible ROs with stage delays of only 5.7 ns. The improved performance of our devices, compared with previous works, could be attributed to the following improvements. First, the ultrahigh semiconducting purity (>99.99%) allowed us to shrink the channel length (~2 μm) and also improve the tube density (~100 tubes per μm) to achieve a high current density (~17.2 μA μm^{-1}) without sacrificing the I_{on}/I_{off} ratio. Second, the high carrier mobility (~50 cm^2 V^{-1} s^{-1}) also helped improve the transistor current density. Third, the reliable CNT NFETs enabled high-performance CMOS logic with high inverter

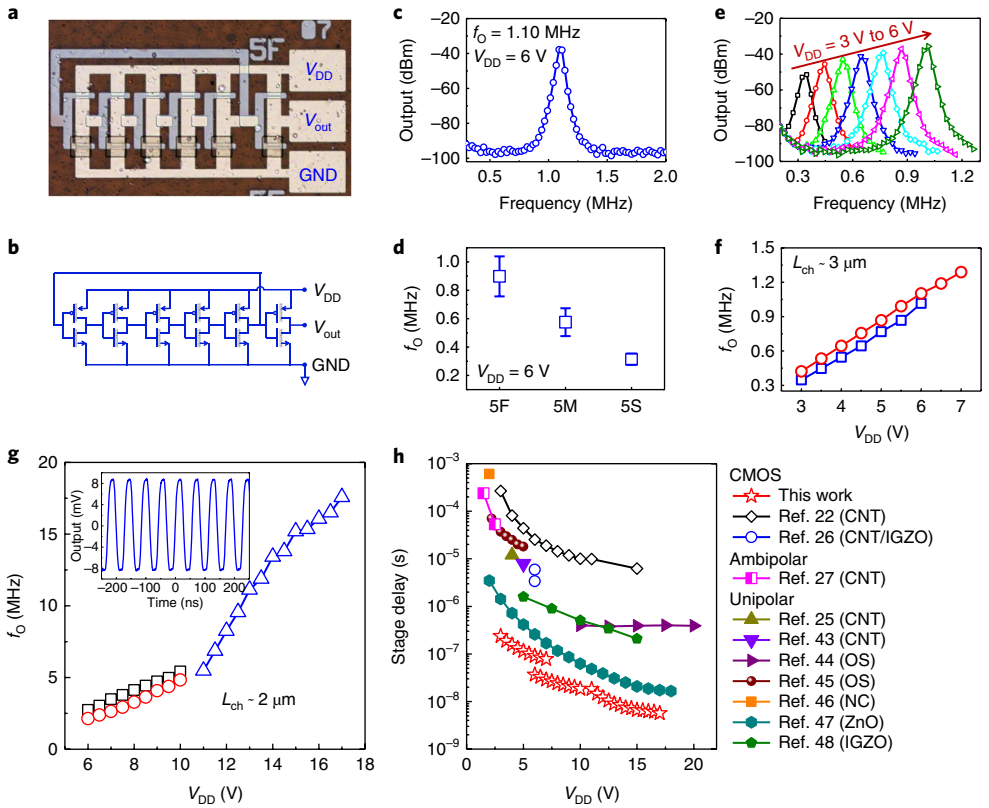

Fig. 4 | Flexible CNT CMOS ROs. a,**b**, Microscope image (**a**) and schematic diagram (**b**) of a five-stage CNT CMOS RO with an additional inverter stage as the output buffer. **c**, Output frequency spectrum of the five-stage CNT RO, showing an oscillation frequency of f_O = 1.10 MHz at a supply voltage of V_{DD} = 6 V. **d**, Output oscillation frequency comparison between ROs with different device dimensions: L_{ch} = 3 µm and L_{ov} = 3 µm for 5F; L_{ch} = 3 µm and L_{ov} = 5 µm for 5M; L_{ch} = 5 µm and L_{ov} = 5 µm for 5S. Error bars represent standard deviations from eight ROs for each device dimension. **e**, Output frequency spectrum of CNT RO at different supply voltages from 3 V to 6 V (in steps of 0.5 V). Both oscillation frequency and amplitude increase with supply voltage. **f**, Dependence of oscillation frequency f_O on supply voltage for two exemplary CNT ROs with L_{ch} = 3 µm. **g**, Improved oscillation frequency for optimized CNT ROs with L_{ch} = 2 µm. Inset: output waveform with f_O = 17.6 MHz at V_{DD} = 17 V. **h**, Comparison of stage delay among representative flexible ROs made with different nanomaterials, including CNTs, organic semiconductors (OSs), oxide semiconductors (IGZO, indium gallium zinc oxide; ZnO), nanocrystals (NCs) and hybrid nanomaterials. Our work shows the smallest stage delay, down to 5.7 ns.

gain and large noise margin. Finally, we designed and fabricated the flexible RO with small source–drain-to-gate overlaps (3–5 µm) to minimize parasitic capacitance, which is shown to have a significant effect on circuit performance. Our flexible RO performance could be further enhanced through additional optimizations, such as scaling down the TFT dimensions, reducing parasitic resistance/capacitance and improving CNT density[32,33]. This work provides a useful approach to build scalable, low-cost and high-speed flexible electronics for practical applications. The performance of our devices and the integration-level demonstration also highlight the potential of using CNT flexible electronics in future applications such as the 'Internet of Things' (IoT) and edge computing.

Methods

Polymer-sorted CNT solution preparation. Semiconducting CNTs were isolated using a polymer extraction technique based on the procedure described in refs [5,6]. A co-copolymer, poly((9,9-dioctylfluorenyl-2,7-diyl)-*alt*-co-(6,6′-(2,2′-bipyridine))) (PFO-BPy, purchased from American Dye Source), was used to selectively extract semiconducting single-walled CNTs (AP-CNT, purchased from Carbon Solutions). PFOBpy (10 mg) was dissolved in 10 ml of toluene with gentle heating (~90 °C) to fully dissolve the polymer. Approximately 20 mg of single-walled CNTs was added to the toluene solution and sonicated with a 6 mm sonication tip (Sonics VCX 250) for 30 min with 1 s pulses while being cooled in a water bath. Following sonication, the solution was centrifuged for 30 min at 30 kr.p.m. in an SW T41 rotor (Beckman). The top 90% of the solution was then collected. This centrifugation process was repeated three more times. The solution was then used as is.

CNT TFT fabrication. CNT TFTs were fabricated on flexible polyimide substrates (DuPont Kapton 300HN and 500HN), which were pre-laminated on a silicon wafer using adhesive polydimethylsiloxane for the purpose of easy handling during sample fabrication. A standard photolithography process was used to first pattern the local back gates, followed by electron-beam evaporation of a 2 nm Ti/50 nm Pd/1 nm Ti stack and then liftoff. The native titanium oxide formed over the top Ti layer acted as a seeding layer for subsequent ALD. The gate oxide stack consisted of 40 nm Al_2O_3/10 nm HfO_2 (by ALD at 150 °C). The HfO_2 capping was critical to help protect the Al_2O_3 layer from attack by the photoresist developer (AZ 400K from MicroChemicals) in the photolithography process. Using a shadow mask, metal–insulator–metal (MIM) capacitors with the same ALD oxide stack were constructed on a polyimide substrate to obtain an equivalent relative dielectric constant of about ε_r = 6.27. The top HfO_2 surface was functionalized with a SAM of chloro(dimethyl)octadecylsilane (Sigma-Aldrich). High-density CNT random networks were deposited on the sample by a standard dropcasting method using the polymer-sorted CNT solution. The receiving substrate was then thoroughly rinsed with toluene and isopropanol. After that, source–drain metal contacts were defined by photolithography and electron-beam evaporation of a 0.2 nm Ti/70 nm Pd stack. Finally, another photolithography and oxygen plasma etching step was used to define the TFT channel region.

CNT CMOS circuit fabrication. For fabrication of CNT complementary circuits, a nominally 2-nm-thick layer of Al was evaporated on the TFT sample, and was readily oxidized into AlO_x in air, then 40 nm Al_2O_3 was deposited by ALD at 150 °C to further enhance the n-type doping. Standard photolithography was used to protect the NFETs, leaving the PFETs open. The AlO_x/Al_2O_3 bilayer passivation on PFETs was then etched away using 50:1 buffered oxide etchant.

Instrumentation. The purified CNT solution was characterized using a UV–vis–NIR absorption spectrometer (Perkin-Elmer Lamda 950). CNT TFTs and inverters

were measured at room temperature on a Cascade Microtech Summit 12000 semi-automated probe station connected to an Agilent B1500A Semiconductor Device Analyzer. CNT ROs were measured using an HP8591A spectrum analyzer and KEYSIGHT InfiniiVision MSOX6004A mixed signal oscilloscope.

Data availability. The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

J.T. conceived and designed the experiments. G.T. prepared the purified CNT solution and deposited CNT thin films. J.T. fabricated the devices and performed the measurements with help from Q.C., K.A.J., L.N., D.B.F. and S.-J.H. J.T. wrote the manuscript. All authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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