EE Times - IBM Nanotubes May Redefine Future of Moore's Law

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Switch to carbon at 3-to-5 nanometer
PORTLAND, Ore.—If a breakthrough in carbon nanotube transistors from IBM Research pans out, the hard stop of 2028 in International Technology Roadmap for Semiconductors (ITRS) is about to get extended. IBM says it has found a way to scale down the channel length to the 1.8 nanometer node (four technology generations away) and beyond to the angstrom level eventually. If they are right, Moore's Law may now be extended to the sub-nanometer angstrom (1/10th of a nanometer) levels using the same extreme-ultraviolet (EUV) complementary metal oxide semiconductor (CMOS) process technologies already in place.

"The 1.2 nanometer wide carbon nanotube channel is already proven," Shu-Jen Han, IBM manager of nanoscale science and technology at its T.J. Watson Research Center (Yorktown, Heights) told EE Times in an exclusive interview. "The major issue for scaling, not only for carbon nanotubes, but for silicon and III-V materials [indium, gallium, arsenide] is the contact—which is no longer scaling."

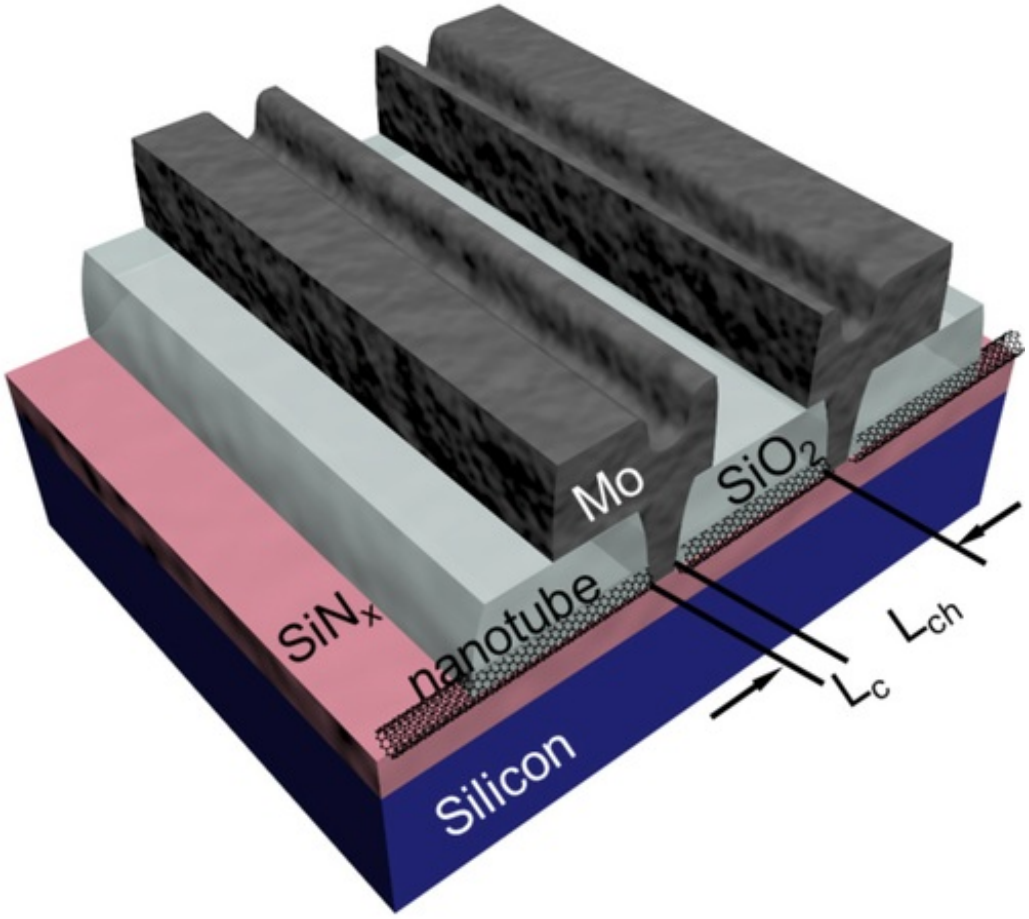
"With our recent breakthrough," said Han, "we now know how to scale [the contact] so it is no longer the limiting factor for carbon nanotube transistors. Our new contacts are measured in angstroms and have just just 36 k-ohms of resistance, including both ends."

The reflection of Roland Germann, manager, Nanotechnology Center Operations at IBM Research - Zurich in the clean room.
(Source: IBM, used with permission)

The breakthrough technique was a long time coming, but according to analyst Richard Doherty, research

director at Envisioneering (Seaford, N.Y.), that was only to be expected.

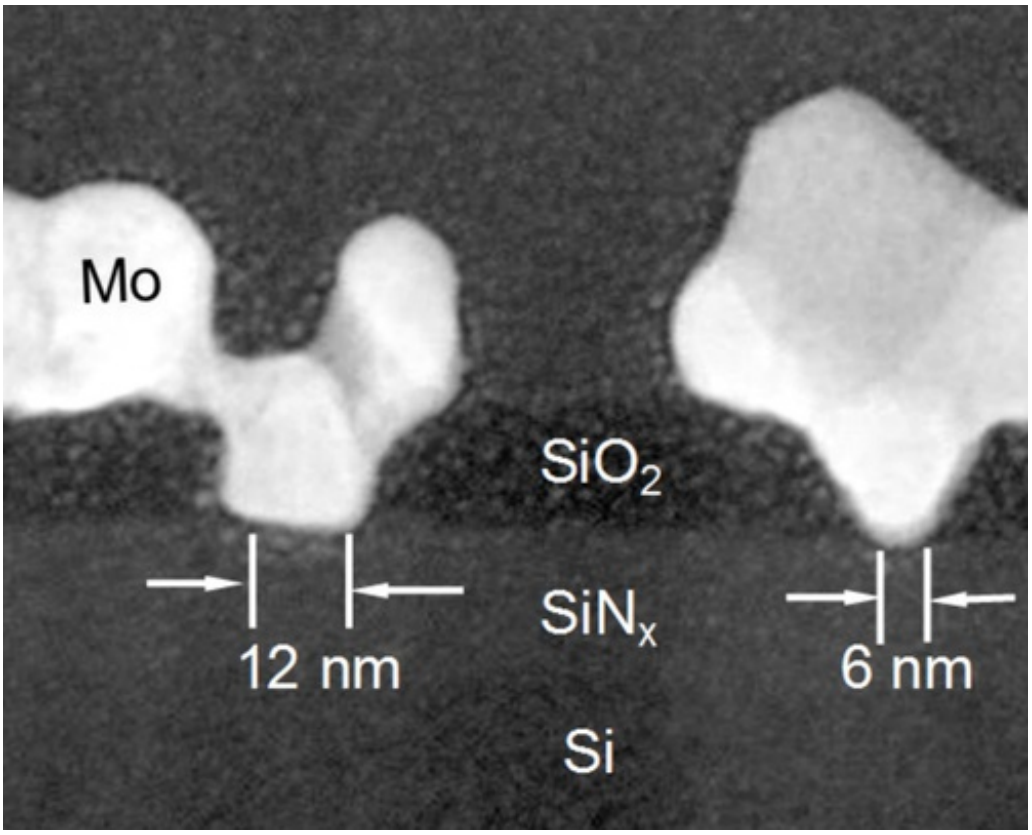
"After all, if you remember that it took about a decade to go from point-contact transistors at Bell Labs to planar transistors at Fairchild and Intel, its not surprising at all that it took IBM a decade too," Doherty told EE Times in an exclusive interview.



Schematic showing the fabricated nanotube transistor with an end-bonded contact and a contact length below 10 nm.
(Source: IBM Research, used with permission)

IBM's proof-of-concept chip has nine-nanometer channels, but before the breakthrough the contacts were giant in comparison. Now IBM has found a way to make smaller contacts enabling them to scale down the channel length to the 1.8 nanometer node (four technology generations away) and beyond to the angstrom level eventually. Each nanotube carries only about 15 microamps, but IBM plans to solve that problem by just using as many nanotube channels in parallel as required for the type of drive a transistor needs for a particular location in a design.

"We can place nanotubes in parallel with about a 8-to-10 nanometer pitch using self aligning techniques," Han revealed to EE Times. "We deposit them using a PVD [physical vapor deposition] process, then use high-temperature annealing--a metallurgical process akin to microscopic welding--to secure the channel contacts at each end."



Cross-sectional transmission electron microscope (TEM) image showing the fabricated nanotube transistor with an end-bonded contact.
(Source: IBM Research, used with permission)

Analyst Doherty was impressed by IBM's "welding" technique and thinks it will give IBM a competitive advantage over the competition. It works by coating the end of the nanotubes with molybdenum before their self-aligned placement as transistor channels. Then the 'welding' step is completed by heating the whole assembly to 1,562 degrees Fahrenheit (850 degrees Celsius) thus melting the molybdenum and chemically transforming it into carbide, a conductor that makes an excellent angstrom-scale contacts.

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"This clever welding/carbide discovery seems to be the only silicon-processing favorable metal without oxidation problems and or Schottky barrier characteristics would add an undesirable step-voltage threshold. Rather IBM's method has an on/off current switching ratio of 10,000, which is great," Doherty told EE Times. "Others trying side connection schemes [to nanotubes] seem to vary in resistance and conductance over time, making them only lab curiosities. IBM's end-cap success paves the way for real nanotube structures that can make use of already proven silicon photolithography techniques.

Schematic showing a fabricated set of devices with different contact geometries on the same nanotube to verify that the contact size can shrink without reducing device performance.
(Source: IBM Research, used with permission)

Today IBM is only able to produce p-type transistors using its revolutionary "welding" technique, but it claims the devices work better than FinFETs and their next step--already under way with light at the end of the tunnel, according to Han--is n-type devises so that CMOS nanotube transistors can be fabricated at the 3-nanometer node by the time silicon FinFETs reach the 5 nanometer node.

"IBM's internal goal is to be ready to come in at the 5-nanometer node and become the best option for the

3-nanometer node all the way down to the angstrom level," Hans told us.

According to Doherty, IBM's achievement gives new hope to extending Moore's Law into the indefinite future, since no insurmountable scaling problems are seen for the nanotube 'welding' technique, which Doherty dubs IBM's coaxial connection technology.

"And succeeding with these coaxial end caps at nine nanometers gives courage and confidence to the industry to there being an alternative semiconductor path as silicon gets more and more inefficient as we push its limits under Moores Law," Doherty told us. "Also I have rarely seen a paper [IBM's Science paper] with so many attributions to other researchers. Their goal is production within a decade, but I am sure they want it faster than that if possible."

IBM's success is a part of its $3 billion research and development effort for post-silicon technologies, started in 2014, to pave the way to the computing needs of what IBM calls the coming "cognitive computing era."

Get all the details in the the Oct. 2nd issue of Science magazine.

— R. Colin Johnson, Advanced Technology Editor, EE Times

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