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TECHNOLOGY UPDATE

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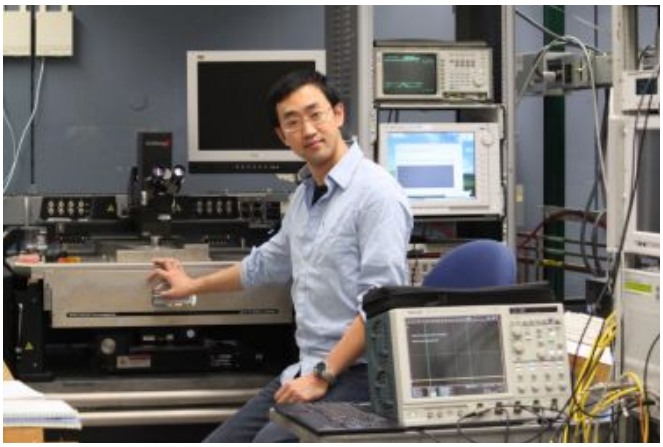
CNTs show feasibility for practical devices

While carbon nanotubes (CNTs) have long attracted interest for nanoscale electronics, practical deployment of the technology requires a level of device consistency that is still a long way from being achieved. Now researchers at IBM in the US have identified the main source of device variability in CNT transistors and ways of reducing it.



(http://images.iop.org/objects/ntw/news/14/2/15/photo.jpg)

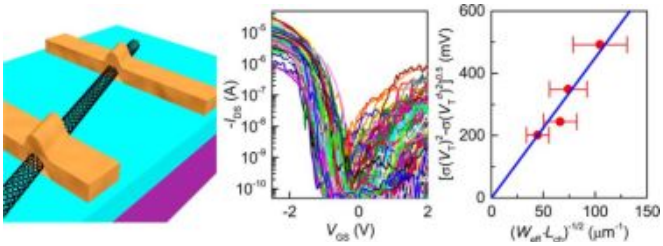
Qing Cao in his lab at IBM, US. (http://images.iop.org/objects/ntw/news/14/2/15/photo.jpg)

In recent years, silicon transistors have been fast approaching their minimum size. Short channel effects and increasing chip power density may halt the trend in constantly decreasing transistor sizes described in 'Moore's Law'. Fortunately, there is an alternative.

"The goal of our research is to develop carbon nanotube transistors into a practical technology that can replace silicon in future generations of high-performance microprocessor chips," says Qing Cao (http://researcher.ibm.com/researcher/view.php?person=us-qcao), who led the IBM research team behind these latest results.

Carbon nanotubes have excellent short channel control, a low resistivity between the CNTs and metal contacts, and transport behaviour that allows much lower power consumption for the same on-current density. However where they have fallen short so far is in the uniformity between CNT devices.

"Ultimately we want to integrate billions of nanotube transistors into functional circuits," says Cao. "To do this, we need good consistency from one transistor to the next, so they can all work together at the same voltage." Their latest study demonstrates that the device variability does not originate from the nanotubes themselves, and that it may be reduced by improved deposition processes and better materials for the dielectric components.



(http://images.iop.org/objects/ntw/news/14/2/15/figure.jpg)

The CNT transistors studied. (http://images.iop.org/objects/ntw/news/14/2/15/figure.jpg)

Finding the root of the problem

The researchers fabricated hundreds of bottom-gated field-effect transistors, each made from a p-channel single-walled CNT with a 10nm HfO2 layer deposited as the gate dielectric. Systematic experiments with the devices identified the amount of variability from device to device. The measurements also confirmed that variation in carbon nanotube diameter was not a dominant source of variability in device performance.

The IBM team then built pairs of devices, where the same nanotube was used as the channel for both transistors. Observations of the performance of device pairs revealed that the dominant source was random, and so likely material-related rather than a systematic process-related contribution. Further analysis indicated that trapped charges fixed at the oxide/air interface were the prime suspect.

"I think the results show that it is possible to build practical circuits based on nanotube transistors, but we still need to reduce the variability by several-fold," Cao tells nanotechweb.org. "We have identified the major source as the oxide surface, not anything intrinsic to the nanotubes, so we think we can make it happen with a better fabrication process."

He suggests that the variability may be reduced by better control over the nanotube source and the deposition process. "The current nanotube solution isn't really electronic grade, so we may introduce charges on the oxide during the nanotube deposition process," says Cao. He also suggests that using high quality dielectrics with no free surface near the nanotube may also help.

From working to working well

Cao describes how far CNT electronics has come in the past few decades. "In the beginning, it was an achievement just to make a few good transistors," he says. The fabrication techniques for these devices are now so advanced that it is possible to fabricate a large enough number of high-quality semiconducting nanotubes to study their random behaviour. He adds, "As it gets closer to becoming a practical technology, the device variability becomes an increasingly important issue."

Next the team will work to try and find where the trapped charges come from, and whether they are mainly from dangling bonds at the oxide surface, damage to the oxide during the fabrication process, or residue left by the nanotube solution do that they can eliminate them.

Full details are reported in *ACS Nano* doi: 10.1021/nn506839p (http://pubs.acs.org/doi/abs/10.1021/nn506839p).

About the author

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