Origins and Characteristics of the Threshold Voltage Variability of Quasiballistic Single-Walled Carbon Nanotube Field-Effect Transistors

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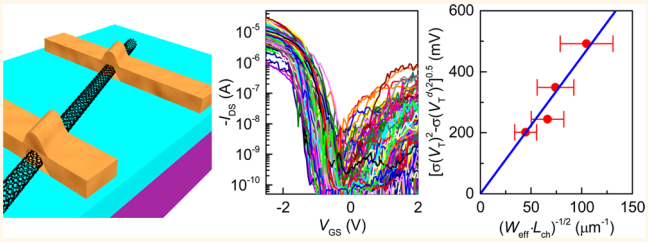
ABSTRACT Ultrascaled transistors based on single-walled carbon nanotubes are identified as one of the top candidates for future microprocessor chips as they provide significantly better device performance and scaling properties than conventional silicon technologies. From the perspective of the chip performance, the device variability is as important as the device performance for practical applications. This paper presents a systematic investigation on the origins and characteristics of the threshold voltage (V_T) variability of scaled quasiballistic nanotube transistors. Analysis of experimental results from variable-temperature measurement as well as gate oxide thickness scaling studies shows that the random variation from fixed charges present on the oxide surface close to nanotubes dominates the V_T variability of nanotube transistors. The V_T variability of single-tube transistors has a figure of merit that is quantitatively comparable with that of current silicon devices; and it could be reduced with the adoption of improved device passivation schemes, which might be necessary for practical devices incorporating multiple nanotubes, whose area normalized V_T variability becomes worse due to the synergic effects from the limited surface coverage of nanotubes and the nonlinearity of the device off-state leakage current, as predicted by the Monte Carlo simulation.



KEYWORDS: carbon nanotube · transistor · threshold voltage · variability

Classical silicon-based metal oxide semiconductor field-effect transistors (MOSFETs) are approaching their scaling limit as the continuous shrinkage of device geometries leads to severe short-channel effects and ever-increasing chip power density.[1] These two limitations could be overcome by replacing the silicon channel with semiconducting single-walled carbon nanotubes (SWNTs).[2,3] The atomically smooth intrinsic ultrathin body of SWNTs offers excellent short channel control even for devices with a gate length less than 10 nm; at the same time, the small width-normalized contact resistivity between SWNTs and metal contacts, which is up to 5 times lower compared to that of state-of-the-art silicon device, as well as the quasiballistic transport of carriers within SWNTs potentially allow the achievement of the same device on-current density under much lower power consumption with reduced device drive voltage.[4,5] Simulation indicates that microprocessors made with nanotube FETs outperform those made on the most advanced silicon technologies by 2−3 times in term of energy-delay product.[6,7]

In addition to performance advantages, to replace silicon, SWNT FETs must have uniformity at least comparable with that of silicon devices with the same dimensions, as the device variability characteristics affect both yield and performance at circuit level. The device threshold voltage (V_T) variability is most critical as it not only directly affects the fluctuation of device off-state leakage current and therefore partially determines the stand-by power consumption of circuits but also significantly influences the variation of device on-state current (I_{ON}) measured under the same operating voltages, which is a critical issue for circuit integrity as it degrades the circuit active performance. Compared to silicon, the absence of dangling

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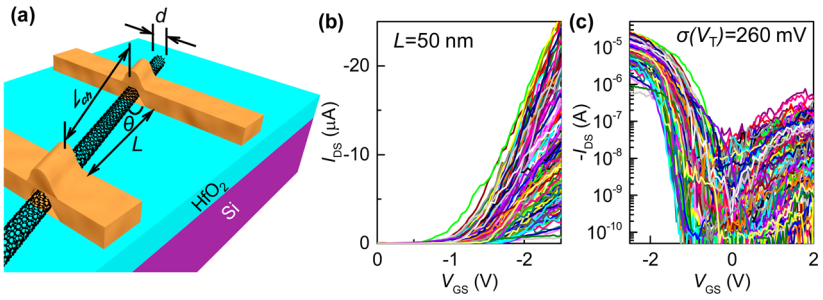

Figure 1. (a) Schematic illustration of an individual SWNT FET constructed on a 10 nm HfO_2/Si substrate. (b, c) Transfer characteristics of a collection of 213 SWNT FETs with *L* of 50 nm in linear (part b) and logarithmic scale (part b), respectively. Applied V_{DS} is −0.5 V.

bond on the surface of nanotubes reduces the formation of fixed charges and traps at the nanotube/high κ dielectric interfaces.[8] In addition, the SWNT channel could be left undoped for both p-channel and n-channel FETs,[9,10] which also helps minimize the V_T variation caused by the random dopant fluctuation. However, the diameter and chirality distributions of nanotubes introduce additional sources of device nonuniformity. Moreover, all atoms of SWNTs are exposed on the surface, which makes nanotubes more susceptible to electrostatic doping by absorbed molecules.[11] In spite of the increasing interest in SWNT FETs, the origins and characteristics of the V_T variability of SWNT transistors, especially for scaled devices operating in quasiballistic regime, have not been experimentally clarified yet.

In this paper, we carried out the first systematic study on the V_T variability of aggressively scaled SWNT FETs, down to ~20 nm channel length (L_{ch}). The origins of V_T variability of SWNT FETs are discriminated through the analysis of experimental results from variable-temperature measurement and gate oxide thickness (t_{ox}) scaling studies. Random fluctuation of the fixed charges present on the gate oxide surface close to SWNTs is identified as the major contributor to V_T variability of quasiballistic nanotube FETs. For the first time, the figure-of-merit from the Pelgrom plot is obtained for the V_T variability of SWNT devices and benchmarked with that of state-of-the-art silicon technologies. Finally, the variability performance of devices incorporating multiple nanotubes per channel is projected based on Monte Carlo simulations. The result suggests that the V_T uniformity of individual nanotube transistors is quantitatively comparable to that of silicon FETs of similar dimension, but still need to be further improved in order to match the variability performance of tube-array devices to that of bulk silicon transistors.

RESULTS AND DISCUSSION

The V_T variability characteristics of SWNT FETs were characterized by measuring the performance of hundreds of individual nanotube transistors made on a wafer with the device structure schematically depicted in Figure 1a. Heavily doped n-type silicon served as the gate electrode to avoid the gate depletion effect for p-channel SWNT FETs, and 10 nm HfO_2 deposited by atomic layer deposition was used as the gate dielectric (κ~13.8 as determined from capacitance−voltage measurement). The bottom gate structure is not only the most widely adopted structure for SWNT FETs in experiments but also scalable for circuit implementations if the bottom gate is not global but locally predefined.[12,13] In addition, since it is much easier to form high-quality dielectrics on a silicon substrate rather than around the surface of nanotubes, the bottom gate structure provides even lower subthreshold swing in experiment compared to that of devices made with the more electrostatically favorable gate-all-around structure.[14,15] Presorted semiconducting enriched SWNTs suspended by sodium cholate in aqueous solution were deposited on the substrate by drop casting. As-deposited SWNTs were then subjected to a vacuum anneal at 450 °C followed by a nitric acid wash to remove surfactant residues from the surface, which improves the device subthreshold swing and the V_T spreading (see Supplementary Figure 1, Supporting Information).[16,17] Source/drain electrodes are Ti/Pd/Au, defined by electron-beam lithography and lift off. Since nanotubes are randomly positioned on the chip, the actual device channel length L_{ch} is approximately calculated as

$$L_{ch} = \frac{L}{\sin\theta} \quad (1)$$

where *L* is the gap between source/drain electrodes and θ is the angle between the axis of the SWNT and the edge of electrodes. Transistors were simply passivated with hexamethyldisilazane (HMDS) before measurement to minimize device hysteresis.[18]

Parts b and c of Figure 1 show the transfer curves of 213 single-nanotube transistors with identically designed *L* of 50 nm, which demonstrate the typical large variations observed in experiments for SWNT FETs. We extract V_T using a constant current criterion, namely the gate bias (V_{GS}) required to achieve a drain-to-source current (I_{DS}) of −100 nA, instead of by extrapolating the slope of transfer curves. This ensures that we define V_T in a regime where the channel resistance is very high, so the influence of parasitic contact resistance is relatively

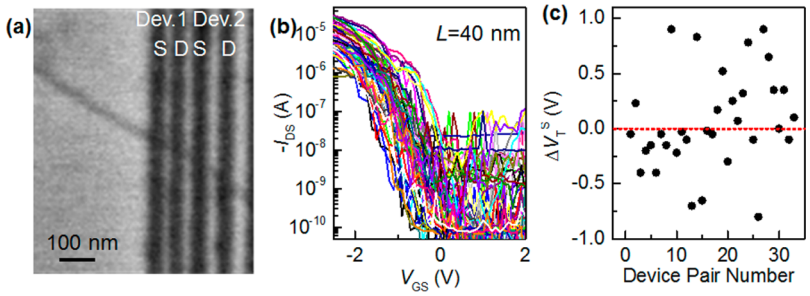

Figure 2. (a) SEM image showing a pair of FETs made next to each other and sharing the same SWNT as channel: S, source; D, drain. (b) Subthreshold plot of transfer characteristics of 66 paired SWNT FETs with *L* of 40 nm. Applied V_{DS} is −0.5 V. (c) Measured ΔV_T^S for each pair.

insignificant.[19] A standard deviation of V_T [$\sigma(V_T)$] around 260 mV is observed.

This large fluctuation could result from contributions from a variety of possible sources, including the differences in nanotube diameter between devices, dopants on nanotubes, the trapped charges at interfaces, and process variations. For a p-type ballistic nanotube transistor, its subthreshold current I_{sth} can be written as

$$I_{sth} \approx \frac{kT}{eR_q}(1 - e^{eV_{DS}/kT})e^{-e(V_{GS} - V_{FB}) - \frac{E_g}{2}/kT} \quad (2)$$

where k is the Boltzmann constant, T is temperature, e is elementary charge, $R_q = h/4e^2$ is the quantum resistance, V_{DS} is the effective drain-to-source bias (reduced by optical phonon scattering), and V_{FB} is the flat-band voltage.[20] E_g is the bandgap of the SWNT which can be calculated as

$$E_g = \frac{2\gamma_0 a_0}{d} \quad (3)$$

where $\alpha_0 = 1.42$ Å is the carbon−carbon bond length, $\gamma_0 = 2.7$ is the nearest neighbor overlap integral, and d is the nanotube diameter.[20] Therefore, V_T defined at a constant off state current I_{th} can be expressed as

$$V_T = V_{FB} - \frac{E_g}{2e} - \frac{kT}{e}\ln\left[\frac{I_{th}eR_q}{kT(1 - e^{eV_{DS}/kT})}\right] \quad (4)$$

Since SWNT devices were fabricated with a polydisperse mixture of nanotubes with various *d*s, diameter distribution contributes to the device V_T variability by affecting the nanotube band structure.[21] To quantify this influence, the exact distribution of d is determined to be 1.2 ± 0.3 nm based on results from both atomic-force microscopy and absorption spectroscopy (see Supplementary Figure 2 and Supplementary Note 1, Supporting Information). The standard deviation of V_T caused by the SWNT diameter variation [$\sigma(V_T^d)$] can then be calculated as

$$\sigma(V_T^d) = \frac{\gamma_0 a_0}{e}\sigma\left(\frac{1}{d}\right) = 88 \text{ mV} \quad (5)$$

which is much smaller than the measured $\sigma(V_T)$ of 260 mV, suggesting that some factors other than the diameter distribution of SWNTs dominate the V_T variability of short channel nanotube transistors. Contributions from other factors to $\sigma(V_T)$, which are treated as independent of d, can be calculated as $[\sigma(V_T)^2 - \sigma(V_T^d)^2]^{1/2}$. Identifying the origins of these factors is critical for us to develop appropriate techniques for the improvement of device variability performance for technology applications.

First, we need to determine whether the observed V_T fluctuation is caused by process-related systematic variability or material-related random variability.[22] Systematic variability originates from the process nonuniformity, and therefore has a long correlation distance. On the other hand, random variability is caused by the discreteness of charge and matter, which shows very short correlation distance. Random variability cannot be eliminated with more precise process control. To distinguish these two types of variations for our fabricated quasi-ballistic nanotube FETs, we built pairs of devices which are not only close to each other in space, but also utilize the same nanotube as the channel as illustrated in Figure 2a. L and contact length for each device are both 40 nm, and the gate dielectric is still 10 nm HfO_2. Figure 2b shows the collection of transfer curves for 66 devices, *i.e.*, 33 pairs, showing that the device V_T spreads over a range of ∼1 V in total. The measured $[\sigma(V_T)^2 - \sigma(V_T^d)^2]^{1/2}$ is 300−420 mV at 95% confidence interval, which incorporates both systematic and random variations. We then calculate the standard deviation of the V_T difference between two neighboring devices in each pair [$\sigma(\Delta V_T^S)$]. Since systematic variations generally have long-range correlation and therefore skew the two V_T values in the same direction, they do not contribute to ΔV_T^S.[23] In addition, as devices in each pair are made on the same SWNT, nanotube diameter variation does not contribute to ΔV_T^S, either. As a result, $\sigma(\Delta V_T^S)$ only evaluates random variability. ΔV_T^S for each pair is plotted in Figure 2c. We can find that ΔV_T^S up to 1 V is observed in several device pairs, showing that the V_T fluctuation caused by random variations could be as large as the total variation between two remotely separated nanotube transistors. The extracted $\sigma(\Delta V_T^S)$ is in the range of 350−580 mV at 95% confidence interval. Therefore, the contribution from random variability to $\sigma(V_T)$ is

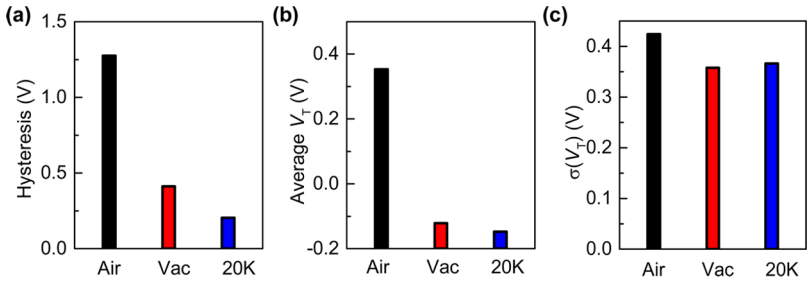

Figure 3. Comparison of device hysteresis (part a), average V_T (part b), and $\sigma(V_T)$ (part c) for a collection of the same 24 SWNT FETs with L of 100 nm fabricated on 10 nm SiO_2/Si substrate measured in air (black), in vacuum after 400 K anneal (red), and at 20 K in vacuum (blue), respectively.

$\sigma(\Delta V_T^S)/\sqrt{2}$ =250−410 mV at 95% confidence interval, which is comparable with the overall $[\sigma(V_T)^2 - \sigma(V_T^d)^2]^{1/2}$ of 300−420 mV. This result indicates that the random variability is the dominant source for device V_T variation of fabricated short-channel SWNT FETs, which is as-expected as no intentional doping process is involved during the nanotube device fabrication flow.

For MOSFETs, random V_T variability could be caused directly by the random nature of both location and number of charges in the active channel or indirectly by the random variations of L_{ch} and t_{ox} as a result of the short channel effects.[24] Since short channel effects are largely suppressed in our nanotube FETs by both scaled dielectric and the extremely thin semiconductor body thickness, with the simulated drain induced barrier lowering for 20 nm channel devices only around 100 mV/V,[25] randomness of charges in device active area, including dopant charges and trapped charges, is most likely the major contributor toward device V_T fluctuation. The trapped charges can be further classified into two major categories. One category of surface traps is associated with the nanotube/oxide interface. They can be charged or discharged by carriers on nanotubes and lead to both the shift of device V_T and the formation of device hysteresis, which is defined as the difference of V_Ts measured from forward and backward sweeps of V_{GS}. They could result from water molecules absorbed on nanotubes or silicon dangling bonds.[26−28] The other category includes those trapped charges that are not in electrical communications with nanotubes, and therefore they are generally termed as fixed charges on interface.[29] They only shift the V_T but do not cause hysteresis. They could originate from excessive amount of one element near the surface of binary oxides,[30] or charged functional groups of some residues left on the surface. Since they are not directly related with the presence of carbon nanotube, it is reasonable to assume that their density is relatively uniform at the oxide/air interface.

To further distinguish which kind of charge is the major source for the V_T variability, we compare the V_T variations measured in air, after a 400 K anneal in vacuum, and at 20 K in vacuum, for the same set of SWNT FETs with L of 100 and 10 nm SiO_2 gate dielectric on p+ silicon substrate (see Supplementary Figure 3, Supporting Information). Applied V_{DS} is −50 mV to avoid the possible influence from the hot electron injection, and V_T is extracted as the V_{GS} required for an I_{DS} of −1 nA. Device hysteresis is measured with the gate voltage swept first from negative to positive and then reversed back. Vacuum anneal removes water molecules absorbed on the surface of nanotubes and, therefore, significantly reduces average device hysteresis as interface traps formed *via* electron injection from nanotubes to attached molecules are largely eliminated, as evident from Figure 3a.[26,27] It also removes some absorbed molecules like oxygen that may dope the SWNTs and negatively shift the device average V_T, which were calculated based on the V_Ts extracted with the V_{GS} swept from negative to positive, as plotted in Figure 3b.[31,32] Low temperature further freezes charge traps caused by imperfect interface between nanotubes and oxide, which suppresses the hysteresis further.[33] However, it does not affect the depletion charge density of SWNTs for such fully depleted devices, and the slightly negatively shifted average V_T is likely caused by the reduction of SWNT Fermi potential with temperature as expected.[34] Here we also notice that the device on-current level is not affected by temperature, which verifies that the majority of fabricated SWNT FETs form ohmic contacts with Pd as most nanotubes have diameters larger than 1 nm.[35−37]

Figure 3c summarizes the change of $\sigma(V_T)$ in response to different environments. Here the $\sigma(V_T)$ is also calculated based on the V_Ts extracted with the negative-to-positive sweep of V_{GS}. Comparing devices measured in air *versus* those measured in vacuum after anneal, $\sigma(V_T)$ is only slightly reduced from 420 mV to ∼360 mV. Such reduction can be explained based on either the decrease of the device doping level as suggested by the shift of average V_T, or the removal of trapped charges caused by absorbed water molecules as suggested by the smaller device hysteresis. However, no additional improvement of $\sigma(V_T)$ is observed at 20 K, even though low temperature reduces the device hysteresis further by 50% through freezing

traps associated with defects at nanotube/oxide interface. These results indicate that these traps that are in direct electrical communications with the semiconducting nanotube channel might contribute to the V_T variability, but their effect seems to be relatively minor compared to that of dopants present around the surface of SWNTs or those fixed charges existing on the gate dielectric surface. Since all devices were made on high quality dielectrics deposited/grown within a semiproduction line at IBM, the fixed charge density within the gate dielectric is very small and should have negligible effects on device V_T variability.

To distinguish whether the V_T variability of SWNT FETs is mainly caused by the random variation of dopants on the nanotube surface or that of fixed charges present at the oxide/air interface, a t_{ox} scaling study was performed. Here we extract both the average V_T and $\sigma(V_T)$ for collections of nominally identical SWNT FETs fabricated on SiO_2 dielectric, with t_{ox} of 2, 3.5, 5, 10, and 15 nm, respectively, grown on n+ silicon substrates. About 100−150 devices were made for each t_{ox}. We first discuss how the average V_T varies as a function of t_{ox}. As shown in eq 4, the V_T of ballistic nanotube FETs can be expressed as

$$V_T = V_{FB} - \frac{E_g}{2e} - \frac{kT}{e}\ln\left[\frac{I_{th}eR_q}{kT(1-e^{eV_{DS}/kT})}\right]$$
$$= \frac{1}{e}(\Phi_M - \Phi_S) - \frac{Q_{SS}}{C_{ox}} - \frac{eN_D}{C_i} - \frac{E_g}{2e} - \frac{kT}{e}\ln\left[\frac{I_{th}eR_q}{kT(1-e^{eV_{DS}/kT})}\right] \quad (6)$$

where Φ_M is the work function of the n+ silicon gate ~4.05 eV, Φ_S is the average work function of nanotube ~4.7 eV,[35] Q_{SS} is the oxide/air interface fixed charge density, and N_D is the dopant concentration. For fixed charges distributed at the dielectric/air interface, the voltage across the oxide is determined by Q_{SS} and the capacitance of a parallel-plate capacitor formed with the planar gate electrode (C_{ox}) according to

$$C_{ox} = \frac{\varepsilon_0\varepsilon_r}{t_{ox}} \quad (7)$$

where ε_0 is the vacuum permittivity and ε_r is the relative dielectric constant of the gate dielectric. On the other hand, for dopants located on the surface of nanotubes, the voltage across the oxide scales with N_D and the gate capacitance of the SWNT (C_i), which can be calculated as[38]

$$C_i = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln(2t_{ox}/d+1)} \quad (8)$$

Figure 4a shows the scaling of the average V_T as a function of t_{ox}. The data can be fitted as either $V_T = (Q_{SS}/\varepsilon_0\varepsilon_r)t_{ox}$ + offset, assuming the oxide surface charge dominates, or $V_T = (eN_D/2\pi\varepsilon_0\varepsilon_r)\ln(2\,t_{ox}/d+1)$ + offset, assuming the dopant charge on the SWNT dominates. Although they both give reasonably good fitting, their

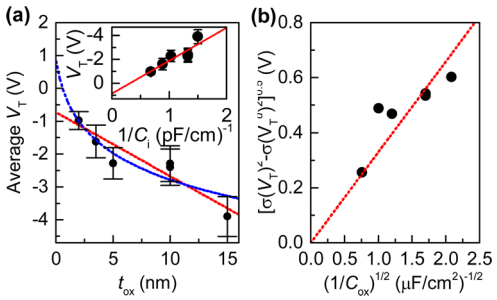

Figure 4. (a) Average V_T of SWNT FETs with L of 100 nm made on SiO_2 gate dielectric as a function of t_{ox}. The blue dotted line shows a fitting to the function of $V_T = A + B[\ln(2t_{ox}/d+1)]^{-1}$, where A and B are fitting parameters. Inset: Average V_T of SWNT FETs as a function of the reciprocal of C_i. (b) The extracted $[\sigma(V_T)^2 - \sigma(V_T^d)^2]^{1/2}$ for devices made on SiO_2 gate dielectric with different t_{ox} as a function of $(1/C_{ox})^{1/2}$. The red dotted lines show linear fits to the data.

y axis intercepts are dramatically different. According to eq 6, the y axis intercept can be calculated as

$$\frac{1}{e}(\Phi_M - \Phi_S) - \frac{E_g}{2} - \frac{kT}{e}\ln\left[\frac{I_{th}eR_q}{kT(1-e^{eV_{DS}/kT})}\right]$$
$$\approx -0.9V \quad (9)$$

However, the scaling of the average V_T with $\ln(2t_{ox}/d+1)$ or C_i^{-1} extrapolates to a very positive y axis intercept (Figure 4a and inset). In addition, if we assume that the effect from dopant charges is important, the value of N_D can be extracted from the slope of linear fitting to Figure 4a inset. The obtained N_D correspond to ~12 holes per 1000 carbon atoms, which is 20 times higher than the doping degree of degenerately doped SWNTs.[39] These results indicate that dopants on nanotubes do not play a major role in determining the V_T of scaled nanotube FETs. On the other hand, linear fitting of the average V_T as a function of t_{ox} or C_{ox}^{-1} suggests a y axis intercept around −0.7 V, which agrees quantitatively well with eq 9. In addition, the Q_{SS} extracted from the slope of the linear fitting to Figure 4a is around 10^{-7} C/cm^2, which is just about an order of magnitude higher than the value reported for pristine SiO_2/air interface as measured by electrostatic force microscopy.[40] This difference could be caused by differences in ambient humidity, the X-ray radiation damages to the oxide surface during e-beam metal deposition, or charged contaminations left on the surface from the nanotube deposition process. We conclude that that the V_T shift and its variability in our SWNT FETs is primarily due to fixed charges distributed at the dielectric/air interface, with at most a small contribution from dopants on nanotubes and other effects discussed earlier.

Next we consider the V_T variations. The classic picture for MOSFETs is that nominally identical devices exhibit different threshold voltages due to the inherent statistical variations in the number of charges per device.[41]

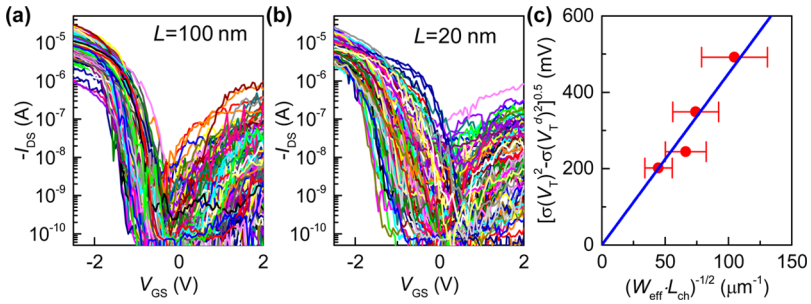

Figure 5. (a, b) Subthreshold plots of transfer characteristics of a collection of 148 SWNT FETs with *L* of 100 nm (part a) and a collection of 117 SWNT FETs with *L* of 20 nm (part b), all made on 10 nm HfO_2/Si substrate. Applied V_{DS} is −0.5 V. (c) Pelgrom plot of SWNT FETs made with 10 nm HfO_2 as gate dielectric, showing the correlation between V_T variability caused by factors other than SWNT diameter distribution $[\sigma(V_T)^2 - \sigma(V_T^d)^2]^{0.5}$ and the effective device area expressed as the product of effective device width (W_{eff}) and length (L_{ch}). See the Supporting Information (Supplementary Note 2) for the detailed descriptions on the calculation of error bars. Solid blue line shows a linear fit to the data.

However, it is unclear how directly this picture can be applied to SWNT FETs. It is well-known that the transport properties are disproportionately affected by charges that are very near the nanotube. Even a single charge, when sufficiently close, can create a potential barrier that substantially changes the device characteristic.[42,43] Because the effect of a charge depends on distance from the tube in a complex way, and the effects of multiple charges are not simply additive, it is not possible to reduce the threshold variability to a simple statistical problem, and a rigorous discussion would be beyond the scope of this paper. We therefore simply adapt the classic picture in a phenomenological way, treating the threshold variations as resulting simply from statistical variations in the number of electrons within an effective device width W_{eff}. Since charges near the nanotube are important, while charges at distances larger than t_{ox} are screened by the gate, the effective device width should scale with t_{ox}, so we write $W_{eff} = \Lambda t_{ox}$. The phenomenological proportionality constant Λ gives some flexibility to weight the relative importance of very close charges in fitting experiment, to compensate for the limitations of our treatment. Note that although only the number of charges within W_{eff} is important in determining the variability, the presence of similar density of electrons out of W_{eff} ensures that on average the electric field corresponds to that of a parallel plate capacitor.

The number of charges within W_{eff} is $n_{SS} = WL_{ch}Q_{SS}/e$, and the standard deviation of n_{SS} $[\sigma(n_{SS})]$ can be calculated as

$$\sigma(n_{SS}) = \sqrt{n_{SS}} = \sqrt{\frac{Q_{SS}}{e} W_{eff} L_{ch}} \qquad (10)$$

assuming n_{SS} distributes with the statistical fluctuation of random process.[23] The V_T variability can then be calculated as

$$\sqrt{\sigma(V_T)^2 - \sigma(V_T^d)^2} = \frac{e}{C_{ox} W_{eff} L_{ch}} \sigma(n_{SS}) \qquad (11)$$

Therefore, $[\sigma(V_T)^2 - \sigma(V_T^d)^2]^{1/2}$ is given as follows

$$\sqrt{\sigma(V_T)^2 - \sigma(V_T^d)^2} = \sqrt{\frac{e}{C_{ox}}} \sqrt{\frac{Q_{SS}}{L_{ch} \varepsilon_0 \varepsilon_r \Lambda}} \qquad (12)$$

which should scale linearly with $(1/C_{ox})^{1/2}$, as illustrated in Figure 4b. The linear fitting extracts Λ to be 0.29 ± 0.02.

Since the data are well described by this simple statistical treatment, including their dependence on L_{ch} and t_{ox}, we can apply the universal equation derived by Pelgrom *et al.*

$$\sigma(V_T)^2 - \sigma(V_T^d)^2 = \frac{A(V_T)^2}{W_{eff} L_{ch}} \qquad (13)$$

to calculate the figure-of-merit $A(V_T)$ characterizing the variability performance of the device.[41] As expected, smaller device active area leads to less averaging effect and therefore more significant device variation as evident from comparing the V_T spread for devices made with *L* of 100 or 20 nm, both on a scaled dielectric of 10 nm HfO_2 (Figure 5a,b). Thus, for long channel devices, effects from such random variations diminish and the V_T fluctuation is dominated by the SWNT diameter distribution.[44] Plotting $[\sigma(V_T)^2 - \sigma(V_T^d)^2]^{1/2}$ as a function of L_{ch} allows us to extract the $A(V_T)$ to be 4.5 ± 0.5 mV·μm for SWNT FETs with linear regression as depicted in Figure 5c. The $A(V_T)$ of our SWNT FETs is comparable with that of the 65 nm node bulk silicon technology,[45] even though the equivalent oxide thickness of our devices is larger, and is about 4 times higher than the best value reported for silicon FETs so far, which employ much thinner high κ oxide as gate dielectric.[24,46] This result is quite encouraging as our SWNT FETs are measured only with a simple HMDS passivation. Improved passivation schemes, together with further scaling of t_{ox}, are expected to further reduce the $A(V_T)$ value, and possibly match the V_T variability characteristics of individual nanotube FETs with that of the most advanced silicon technologies.

Even though scaled single-tube FETs match their normalized V_T variability performance with that of

current silicon transistors, for practical applications we cannot construct circuits based on such single tube transistors. Realistic FETs must incorporate multiple nanotubes as the channel to increase the output current and reduce the V_T spreading. In the final part of this paper, we will predict the variability characteristics for multiple tube FETs based on the measured performance of individual nanotube transistors. Since the device off-state leakage current is exponentially proportional to the gate overdrive voltage, defined as the difference between gate voltage and V_T, the V_T of multiple-tube device is determined by the single-tube component with the minimum V_T within the transistor, instead of their algebraic average.[47] Therefore, $\sigma(V_T)$ of the device will not scale with the number of nanotubes in the channel (N) following the $1/\sqrt{N}$ rule as predicted by the central limit theorem, but rather will converge to a Gumbel distribution according to the Fisher–Tippett–Gnedenko theorem.[48]

The dependence of $\sigma(V_T)$ on N is evaluated numerically with the Monte Carlo simulation. In each sample device, N V_T values were randomly selected from a pool of measured V_Ts of single-tube FETs with L of 20 nm, whose distribution is shown in Figure 6a. The simulated V_T of this sample device is then defined as the highest (least negative) of these N V_T values. Ten thousand samples were generated for each N number, and the calculated $\sigma(V_T)$ for multiple tube devices as a function of N is plotted in Figure 6b. It shows that the $\sigma(V_T)$ reduces at a rate slower than $1/\sqrt{N}$, and therefore, the Pelgrom plot cannot be used to describe how the V_T variability scales with device width N for multiple tube FETs. Assuming a nanotube pitch of 8 nm for SWNT arrays, $\sigma(V_T)$ for devices with a width of 180 nm ($N = 23$), *i.e.*, standard device width for FETs in 22 nm technology node, is about 150 mV, which is 3–5 times larger than that of silicon devices with an identical geometry. It means that $\sigma(V_T)$ for individual nanotubes has to be reduced from ~500 to 100–160 mV in order to make the variability performance of multiple-tube FETs match that of silicon devices. The development of passivation schemes better than HMDS coating which have the capability to reduce Q_{SS} further by at least 10 times is necessary to meet this target. We also analyze the variability performance of I_{ON} for multiple tube devices. Here we use the same V_{GS} so it includes contributions from V_T variability, the nanotube diameter variation,[20] and the fluctuations caused by the parasitic contact resistance. Again in each sample device, N I_{ON} values were randomly selected from a pool of measured I_{ON}s of single-tube FETs with L of 20 nm, whose distribution is shown in Figure 6c. We assume each nanotube inside the array operates independently and I_{ON} of the device is then expressed as the sum of currents flowing through each SWNT. Ten thousand samples were generated for each N number. The simulated correlation between the

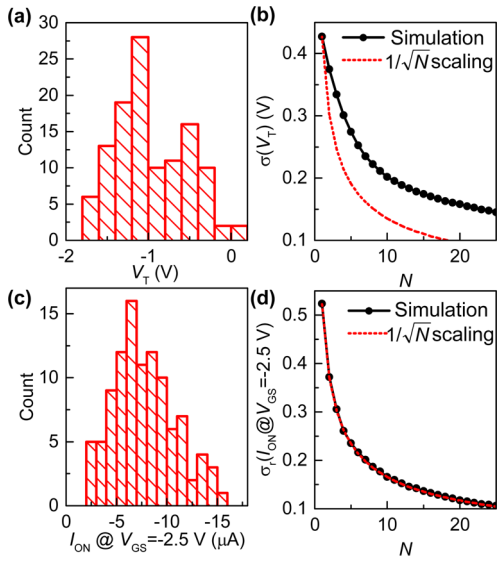

Figure 6. (a) Histogram showing the distribution of V_T for SWNT FETs with L of 20 nm. (b) The change of $\sigma(V_T)$ with the number of SWNTs within each device (N) simulated using the Monte Carlo method (black) and its deviation from the $1/\sqrt{N}$ scaling (red dotted lines), respectively. (c) Histogram showing the distribution of saturation I_{ON} measured under identical V_{GS} of −2.5 V ($I_{ON}@V_{GS}$=-2.5 V) and I_{DS} of −0.5 V for SWNT FETs with L of 20 nm. (d) Change of $\sigma_r(I_{ON})$ measured under identical V_{GS} of −2.5 V [$\sigma_r(I_{ON}@V_{GS}$=-2.5 V), black] for SWNT FETs with L of 20 nm as a function of N as simulated by the Monte Carlo method (black) and predicted by the $1/\sqrt{N}$ scaling (red dotted lines), respectively.

relative standard deviation of multiple tube device I_{ON} [$\sigma_r(I_{ON})$] and N is illustrated in Figure 6d, which follows the $1/\sqrt{N}$ rule as expected. Therefore, for an array with 8 nm pitch, devices based on SWNTs will demonstrate I_{ON} variability comparable to that of silicon devices.[19] Further tightening of V_T variability and the fluctuation of contact resistance will continue improving the I_{ON} variation of scaled SWNT transistors.

CONCLUSIONS

In conclusion, systematic studies of the variability of quasi-ballistic SWNT FETs show that random fluctuation of fixed charges on the oxide/air interface is the major source for device V_T fluctuation of bottom gated SWNT transistors. A Pelgrom plot shows that the $A(V_T)$ of single-tube FETs is comparable with that of silicon technologies. Further reduction of $A(V_T)$ is expected to result from the scaling of dielectric thickness. The variability performance of devices based on multiple nanotubes is projected using the Monte Carlo simulation. The result indicates that the I_{ON} variability performance of SWNT FETs becomes comparable to that of silicon devices after introducing multiple tubes as the channel. However, the V_T variability performance of multiple tube devices could be much worse than that of current silicon devices, even though SWNT FETs demonstrate comparable V_T variability on single-tube level, due to the synergic effects from the nonlinearity

of the device off-state leakage current and the existence of certain pitch among nanotubes. Better passivation schemes to reduce the interface fixed charges, improved sorting or synthesis techniques to minimize nanotube diameter distribution,[49−51] together with novel assembly techniques to reduce the pitch among nanotube arrays,[52,53] are likely required to further improve the variability performance of devices based on multiple-tube arrays and make SWNT logic electronics a practical technology.

METHODS

Processing of Nanotubes. An aqueous solution of SWNTs was prepared by dispersing nanotube powders synthesized by arc-discharge method (Hanwha Nanotech, ASP-100F) in a 1 wt % solution of sodium dodecyl sulfate (SDS) *via* horn sonication (20 min, 1 s pulse, 600 W, 99% amplitude, 20 kHz). The solution was further purified with a step-gradient centrifuge step using 45% iodixinol (Sigma-Aldrich) solution with 0.25% SDS as a stopping layer at 287700 g for 15 h with the help of a Beckman Coulter Optima L-100 XP ultracentrifuge with a swinging bucket type rotor to remove graphitic impurities and large bundles. Semiconducting enriched nanotubes were further separated from the purified solution by means of column chromatography according to previously reported method.[54]

Device Fabrication. The sorted nanotube solution was further diluted by ∼20× with 1 wt % sodium cholate solution and was sonicated again with a bath sonicator for 10 min before use. A few drops of SWNT solution were deposited to the target substrate, allowed to sit for 5 min, and then blown dry with nitrogen. Excess surfactants were removed first with a gentle methanol wash followed by a vacuum anneal with base pressure less than 10^{-6} Torr at 450 °C for 2 min. The remaining amorphous carbon was removed by soaking the substrate into concentrated nitric acid for 2 min. Device source/drain electrodes 15 μm wide were defined by a standard electron beam lithography step followed by lift-off of e-beam evaporated Ti (0.2 nm) /Pd (10 nm)/Au (10 nm). Finally, the chips were placed into a glass desiccator filled with desiccant along with a 2 mL solution of HMDS (Sigma-Aldrich) in an open glass vial. The desiccator was then evacuated using house vacuum. The sealed desiccator was then put in an oven at 150 °C and kept for ∼1 h. After deposition, the samples were cooled, and the devices were tested in air using a semiautomated probe station at room temperature or in vacuo using a manual probe with an Agilent parameter analyzer B1500.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: AFM and absorption measurements to determine the nanotube diameter distribution. Transfer characteristics of a collection of devices measured in air, in vacuum after anneal, and at 20 K in vacuum. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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